R6766-21

RCSCP2 Speech Codec Processor

Designer's Guide

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CONEXANT™

Ordering Information

Factory Part Number	Package	Supported Speech Codecs (***Bit Rate***)								Acoustic Interfaces			
		G.723.1 *(6.4/5.3 kbps)*	**G.723.1 Annex A** *(≅3 kbps)*	**G.711 μ-law** *(64 kbps)*	**G.711 A-law** *(64 kbps)*	**G.728** *(16 kbps)*	**G.729** *(8 kbps)*	**G.729 Annex B** *(≅4 kbps)*	**Digi Talk** *(8.5 kbps)*	**FDSP (with AEC)**	**HDSP**	**Handset (with HEC)**	**Headset**
R6766-21	144-pin TQFP	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Document Revision History

Revision	Date	Comments
A	01/29/99	Initial release

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1. INTRODUCTION

1.1 SUMMARY

The Rockwell RCSCP2 Speech Codec Processor provides bi-directional compressed digital speech. The RCSCP2 supports mandatory and optional speech codecs for ITU video conferencing (H.32x), as well as digital simultaneous voice and data (V.70).

The RCSCP2 can also operate in full-duplex speakerphone (FDSP) mode using acoustic echo cancellation (AEC) concurrently with ITU-T G.723.1, ITU-T G.711 µ-law, ITU-T G.711 A-law, ITU-T G.728, ITU-T G.729, or Rockwell's DigiTalk codec operation. This hardware audio accelerator also includes an analog front end.

When used with Rockwell's modem (e.g., V.90/K56flex™ or V.34) and video capture (e.g., Bt848) devices, the RCSCP2 provides seamless integration of video capture, high-speed data/fax modem, and full-duplex speech. This enables a hardware accelerated H.32x conferencing system utilizing host-based video compression.

The functions supported by the RCSCP2 are summarized in Table 1-1.

Table 1-1. RCSCP2 Supported Codecs and Acoustic Interfaces

Factory Part Number	Package	Supported Speech Codecs (***Bit Rate***)								Acoustic Interfaces			
		G.723.1 *(6.4/5.3 kbps)*	**G.723.1 Annex A** *(≅3 kbps)*	**G.711 µ-law** *(64 kbps)*	**G.711 A-law** *(64 kbps)*	**G.728** *(16 kbps)*	**G.729** *(8 kbps)*	**G.729 Annex B** *(≅4 kbps)*	**Digi Talk** *(8.5 kbps)*	**FDSP (with AEC)**	**HDSP**	**Handset (with HEC)**	**Headset**
R6766-21	144-pin TQFP	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

1.2 FEATURES

- Supported speech codecs
  - ITU-T G.723.1
  - ITU-T G.723.1 Annex A
  - ITU-T G.711 μ-law
  - ITU-T G.711 A-law
  - ITU-T G.728
  - ITU-T G.729
  - ITU-T G.729 Annex B
  - DigiTalk
- Full-duplex speakerphone (FDSP) operation
  - Acoustic echo cancellation (AEC) with echo span up to 128 ms
  - Speaker volume control
  - Microphone gain selection
  - Microphone automatic gain control (AGC)
- Patented robust timing recovery
- Burst data transfer to accommodate operating system latency
- Handset operation with handset echo cancellation (HEC)
- Headset operation
- Programmable functions
  - Host interface memory interrupt functions
  - General purpose input/output pins
- TTL and CMOS compatible
- +5V operation
- 144-pin TQFP package

1.3 APPLICATION EXAMPLES

Figure 1-1 shows the RCSCP2, Bt848 Video Capture ASIC, and RC56D Modem interfacing to a PCI Bus. The RCSCP2 carries out audio/speech encoding and decoding operations in any of the supported speech codec configurations. The Bt848 performs composite video capture up to 30 frames/sec. The RC56D Modem, with the Microcomputer Unit (MCU) packaged in an 80-pin PQFP and the Modem Data Pump (MDP) packaged in a 100-pin PQFP, supports high speed data (V.90/K56flex receive rates up to 56 Kbps and V.34 send rates), high speed fax, DSVD, speakerphone, and voice/audio operation. Downloadable architecture allows upgrading of RC56D modem controller firmware and modem data pump code from the host.

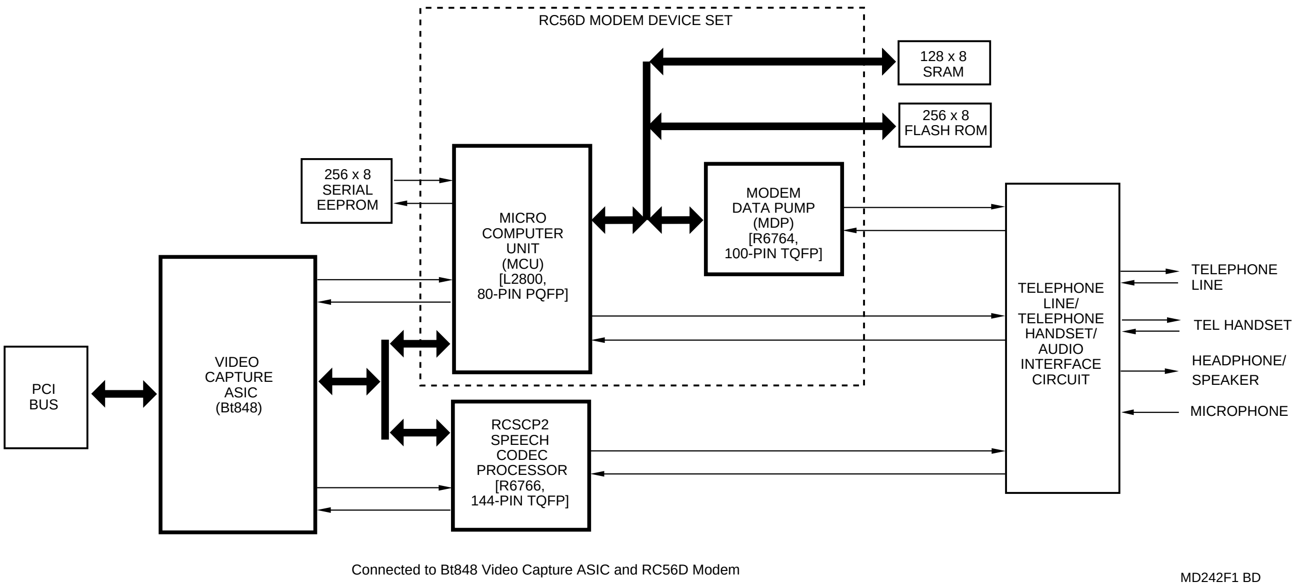

Figure 1-1. Block Diagrams - Typical RCSCP2 Applications

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2. HARDWARE INTERFACE

2.1 HARDWARE SIGNALS

The hardware interface signals for the RCSCP2 in 144-pin TQFP are shown in Figure 2-1.

The pin assignments for the RCSCP2 in 144-pin TQFP are shown in Figure 2-2 and are listed in Table 2-1.

The RCSCP2 hardware interface signals are defined in Table 2-2.

The digital electrical characteristics for the hardware interface signals are listed in Table 2-3.

The analog electrical characteristics for the hardware interface signals are listed in Table 2-4.

The current and power requirements are listed in Table 2-5.

The absolute maximum ratings are listed in Table 2-6.

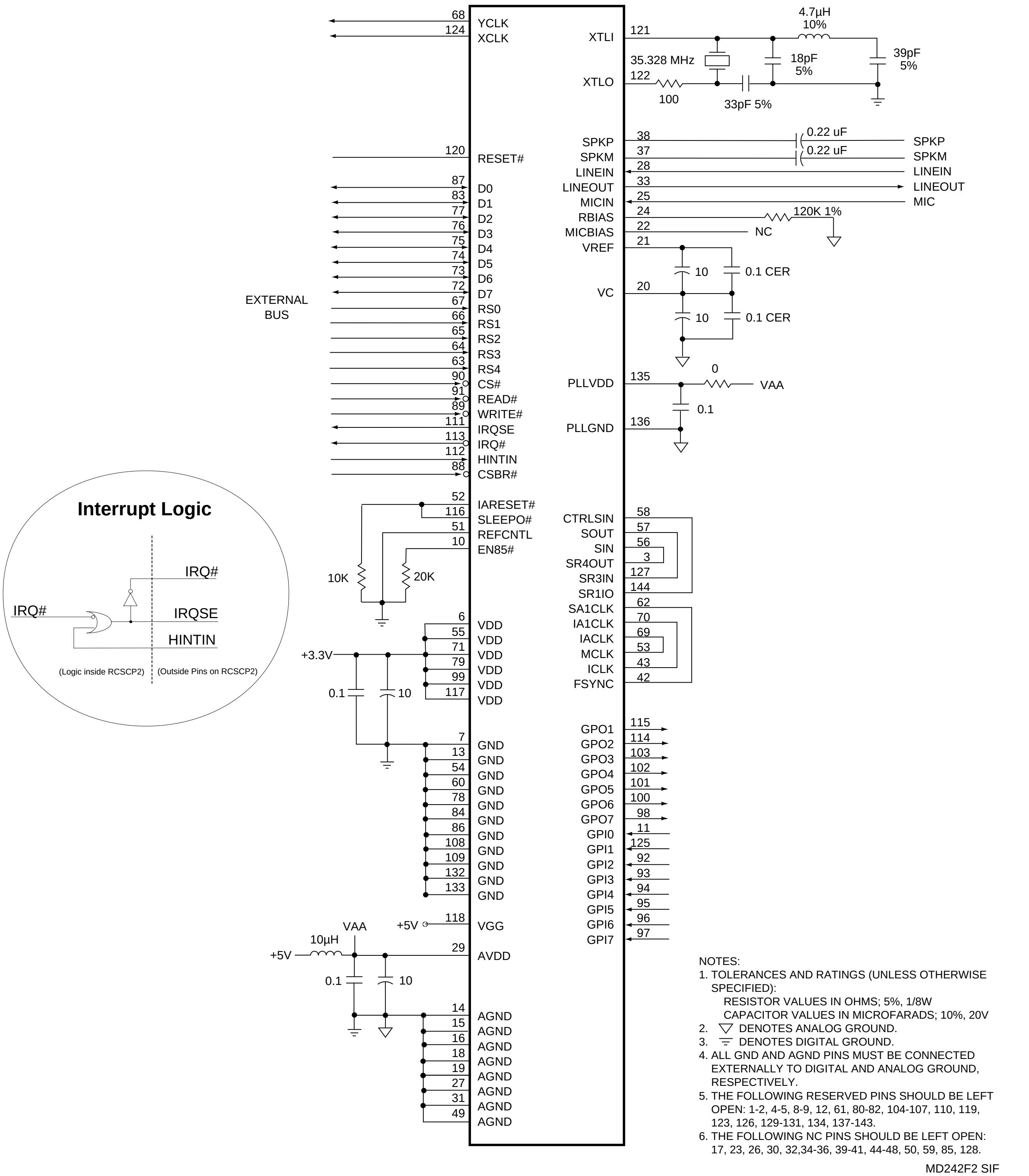

Figure 2-1. RCSCP2 Hardware Interface Signals

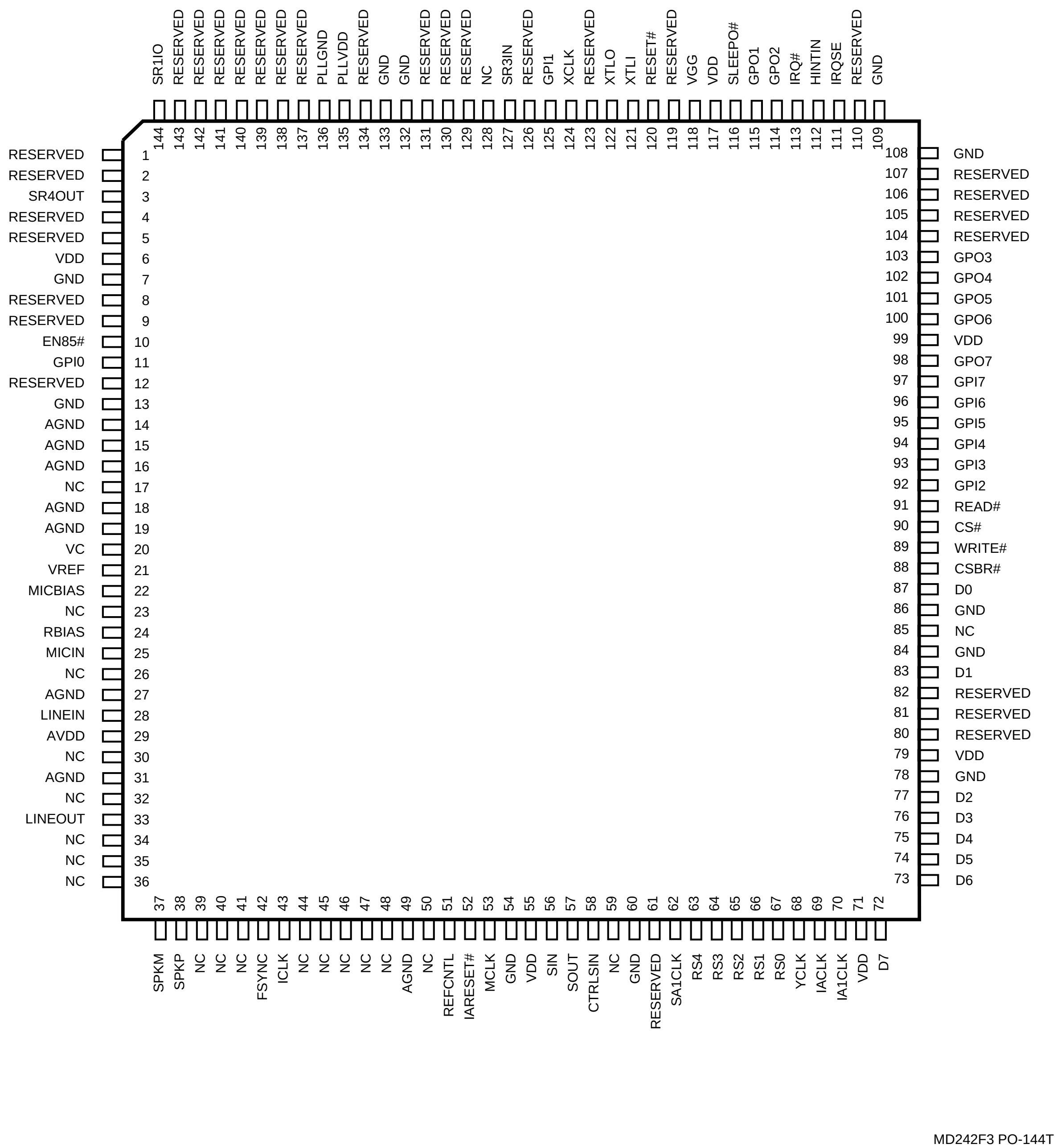

Figure 2-2. RCSCP2 Pin Signals- 144-Pin TQFP

Table 2-1. RCSCP2 Pin Signals - 144-Pin TQFP

Pin	Signal Label	I/O Type	Interface[3]	Pin	Signal Label	I/O Type	Interface
1	RESERVED		NC	73	D6	IB/OC	EB: D6
2	RESERVED		NC	74	D5	IB/OC	EB: D5
3	SR4OUT	DI	To SIN	75	D4	IB/OC	EB: D4
4	RESERVED		NC	76	D3	IB/OC	EB: D3
5	RESERVED		NC	77	D2	IB/OC	EB: D2
6	VDD	PWR	+3.3V	78	GND	GND	GND
7	GND	GND	GND	79	VDD	PWR	+3.3V
8	RESERVED		NC	80	RESERVED		NC
9	RESERVED		NC	81	RESERVED		NC
10	EN85#	IA	GND through 20K ohms	82	RESERVED		NC
11	GPI0	IA	NC	83	D1	IB/OC	EB: D1
12	RESERVED		NC	84	GND	GND	GND
13	GND	GND	GND	85	NC		NC
14	AGND	GND	AGND	86	GND	GND	GND
15	AGND	GND	AGND	87	D0	IB/OC	EB: D0
16	AGND	GND	AGND	88	CSBR#	IB	EB: ~CS
17	NC		NC	89	WRITE#	IB	EB: ~WRITE
18	AGND	GND	AGND	90	CS#	IB	EB: ~CS
19	AGND	GND	AGND	91	READ#	IB	EB: ~READ
20	VC	REF	AGND and to VREF through capacitors	92	GPI2	IA	NC
21	VREF	REF	VC through capacitors and bead	93	GPI3	IA	NC
22	MICBIAS	REF	Leave open.	94	GPI4	IA	NC
23	NC		NC	95	GPI5	IA	NC
24	RBIAS	REF	AGND through 120K ohms	96	GPI6	IA	NC
25	MICIN	I(DA)	T/A IF: MICV	97	GPI7	IA	NC
26	NC		NC	98	GPO7	OC	NC
27	AGND	GND	AGND	99	VDD	PWR	+3.3V
28	LINEIN	I(DA)	T/A IF: TELIN	100	GPO6	OC	NC
29	AVDD	PWR	+5V through filter	101	GPO5	OC	NC
30	NC		NC	102	GPO4	OC	NC
31	AGND	GND	AGND	103	GPO3	OC	NC
32	NC		NC	104	RESERVED		NC
33	LINEOUT	O(DD)	T/A IF: TELOUT	105	RESERVED		NC
34	NC		NC	106	RESERVED		NC
35	NC		NC	107	RESERVED		NC
36	NC		NC	108	GND	GND	GND
37	SPKM	O(DD)	Speaker Circuit	109	GND	GND	GND
38	SPKP	O(DD)	Speaker Circuit	110	RESERVED		NC
39	NC		NC	111	IRQSE	OB	Host IRQ input
40	NC		NC	112	HINTIN	IA	Modem IRQ output
41	NC		NC	113	IRQ#	OA	Host IQR# input
42	FSYNC	DI	To SA1CLK	114	GPO2	OC	NC
43	ICLK	DI	To IA1CLK	115	GPO1	OC	NC
44	NC		NC	116	SLEEPO#	OC	To IARESET#
45	NC		NC	117	VDD	PWR	+3.3V
46	NC		NC	118	VGG	PWR	+5V
47	NC		NC	119	RESERVED		NC
48	NC		NC	120	RESET#	IB	Host Reset
49	AGND	GND	AGND	121	XTLI	I	Crystal In
50	NC		NC	122	XTLO	O	Crystal Out
51	REFCNTL	REF	To AGND	123	RESERVED		NC
52	IARESET#	DI	To SLEEPO# and to GND through 10K ohms	124	XCLK	OB	
53	MCLK	DI	To IACLK	125	GPI1	IA	NC
54	GND	GND	GND	126	RESERVED		NC
55	VDD	PWR	+3.3V	127	SR3IN	DI	To SOUT
56	SIN	DI	To SR4OUT	128	NC		NC

Table 2-1. RCSCP2 Pin Signals - 144-Pin TQFP (Continued)

Pin	Signal Label	I/O Type	Interface3	Pin	Signal Label	I/O Type	Interface
57	SOUT	DI	To SR3IN	129	RESERVED		NC
58	CTRLSIN	DI	To SR1IO	130	RESERVED		NC
59	NC		NC	131	RESERVED		NC
60	GND	GND	GND	132	GND	GND	GND
61	RESERVED		NC	133	GND	GND	GND
62	SA1CLK	DI	To FSYNC	134	RESERVED		NC
63	RS4	IB	EB: A4	135	PLLVDD	PWR	To AGND through 0.1 µF and to VAA through a 0 ohm resistor.
64	RS3	IB	EB: A3	136	PLLGND	GND	To AGND
65	RS2	IB	EB: A2	137	RESERVED		NC
66	RS1	IB	EB: A1	138	RESERVED		NC
67	RS0	IB	EB: A0	139	RESERVED		NC
68	YCLK	OB		140	RESERVED		NC
69	IACLK	DI	To MCLK	141	RESERVED		NC
70	IA1CLK	DI	To ICLK	142	RESERVED		NC
71	VDD	PWR	+3.3V	143	RESERVED		NC
72	D7	IA/OB	EB: D7	144	SR1IO	DI	To CTRLSIN

Notes:

1. I/O types:
   - DI = Device interconnect.
   - IA, IB, IC, ID = Digital input (see Table 2-3).
   - OA, OB, OC = Digital output (see Table 2-3).
   - I(DA) = Analog input (see Table 2-4).
   - O(DD), O(DF) = Analog output (see Table 2-4).
   - MI = Modem interconnect
   - I = Analog input
   - O = Analog output
   - PWR = Power
   - GND = Ground

2. Interface:
   - NC = No external connection allowed.
   - EB = Host external bus.
   - T/A = Telephone/audio interface.

Table 2-2. RCSCP2 Pin Signal Definitions

Label	I/O Type	Signal/Definition
OVERHEAD SIGNALS		
XTLI, XTLO	I/O	**Crystal In and Crystal Out.** The device must be connected to an external crystal circuit consisting of a 35.328 MHz crystal.
RESET#	IB	**Reset.** After application of +3.3V power to the device, RESET# must be held low for at least 15 ms after the +3.3V power reaches operating range. The device is ready to use 25 ms after the low-to-high transition of RESET#. The reset sequence initializes the device interface memory to default values.
IARESET#	MI	**IA Reset.** Connect to SLEEPO#.
VGG	PWR	**5V Supply Voltage for DSP Digital Circuits.**
VDD	PWR	**Digital Supply Voltage for Digital Circuits.** Connect to +3.3V.
AVDD	PWR	**5V Supply Voltage for IA Analog Circuits.** Connect to VCC through decoupling circuit.
GND	GND	**Ground for Digital Circuits.** Connect to digital ground.
AGND	GND	**Analog Ground.** Connect to analog ground.
MICROPROCESSOR BUS INTERFACE		
Address, data, control, and interrupt hardware interface signals allow connection to an 8085 or 6500 bus compatible microprocessor. With the addition of external logic, the interface can be made compatible with a wide variety of other microprocessors, such as the 8080 or 68000. The microprocessor interface allows a microprocessor to change device configuration, read or write channel and diagnostic data, and supervise device operation by writing control bits and reading status bits. **Note:** The device should not be continuously selected for read operation. Also, read or write operations should be delayed by at least 2 XCLK cycles from a preceding write cycle.		
D0–D7	IB/OC	**Data Lines.** Eight bi-directional data lines (D0–D7) provide parallel transfer of data between the host and the device. The most significant bit is D7. Data direction is controlled by the Read Enable (READ#) and Write Enable (WRITE#) signals. During a read cycle, data from the DSP interface memory register is gated onto the data bus via three-state drivers in the DSP. These drivers force the data lines high for a one bit, or low for a zero bit. When not read, the three-state drivers assume their high-impedance (off) state. During a write cycle, data from the data bus is copied into the selected DSP interface memory register, with high and low bus levels representing one and zero bit states, respectively.
RS0–RS4	IB	**Register Select Lines.** Five active high Register Select inputs (RS0–RS4) address interface memory registers within the DSP when CS# is low. These lines are typically connected to address lines A0-A4. When selected by CS# low, the DSP decodes RS0 through RS4 to address one of 32 8-bit internal interface memory registers (00-1F). The most significant address bit is RS4 while the least significant address bit is RS0. The selected register can be read from, or written into, via the 8-bit parallel data bus (D0–D7).
CS#	IB	**Chip Select.** The active low CS# input selects and enables the DSP for parallel data transfer between the DSP and the host over the microprocessor bus.
CSBR#	IB	**Chip Select Buffer RAM.** Active low chip select used when CS# is active to select Interface Memory (CSBR# high) or Buffer RAM (CSBR# low).

Table 2-2. RCSCP2 Pin Signal Definitions (Continued)

Label	I/O Type	Signal/Definition
READ#	IB	**Read Enable.** When EN85# is low (8085 bus selected), reading is controlled by the host pulsing READ# input low during the microprocessor bus access cycle. The read timing is: **Parameter Symbol Min. Max. Units** CS# Setup Time TCS 0 – ns RSi Setup Time TRS 10 – ns Data Access Time TDA – 45 ns Data Hold Time TDHR 10 – ns Control Hold Time THC 10 – ns **Notes:** CS# and READ# must not both be continuously active. A read or write operation following a read operation must be delayed by at least 2 XCLK cycles.
WRITE#	IB	**Write Enable.** When EN85# is low (8085 bus selected), writing is controlled by the host pulsing WRITE# input low during the microprocessor bus access cycle. The write timing is: **Parameter Symbol Min. Max. Units** CS# Setup Time TCS 0 – ns RSi Setup Time TRS 10 – ns Control Hold Time THC 10 – ns Write Data Setup Time TWDS 20 – ns Write Data Hold Time TDHW 10 – ns **Note:** A read or write operation following a write operation must be delayed by at least 2 XCLK cycles.
HINTIN	IA	**External Device Interrupt Request Input.** (Refer to Figure 2-1.) Active high interrupt request, typically from a modem device. An external pull-down resistor is required to prevent spurious interrupt activity on the IRQ# and IRQSE pins.
IRQ#	OB	**RCSCP2 Interrupt Request.** Connect to the host active low input. (Refer to Figure 2-1.) The IRQ# interrupt request output may be connected to the host processor interrupt request input in order to interrupt host program execution for immediate RCSCP2 service. The IRQ# output can be enabled in DSP interface memory to indicate immediate change of conditions in the RCSCP2. The use of IRQ# is optional depending upon the application. The IRQ# output structure is an open-drain field-effect-transistor (FET). The IRQ# output can be wire-ORed with other IRQ# lines in the application system. Any of these sources can drive the host interrupt input low, and the host interrupt servicing process normally continues until all interrupt requests have been serviced (all IRQ# lines have returned high). Because of the open-drain structure of IRQ#, an external pull-up resistor to VDD is required at some point on the IRQ# line. The resistor value should be small enough to pull the IRQ# line high when all IRQ# drivers are off (it must overcome the leakage currents). The resistor value should be large enough to limit the driver sink current to a level acceptable to each driver. If only the IRQ# output is used, a resistor value of 5.6K ohms, 20%, 0.25 W, is sufficient.
IRQSE	OA	**RCSCP2 and External Device Interrupt Request.** (Refer to Figure 2-1.) Active high interrupt request reflecting logical OR of RCSCP2 Interrupt Request and inverted External Device Interrupt Request Input (HINTIN). Connect to the host active high input. IRQSE is active high and is driven at all times other than during Reset.
TELEPHONE LINE/AUDIO INTERFACE		
MICIN	I(DA)	**Microphone In.** MICIN is a single-ended input from the audio interface circuit for routing from microphone input.
SPKP SPKM	O(DF) O(DF)	**Speaker Out Positive, Speaker Out Negative.** These pins are a differential output to the audio interface for routing to a speaker. SPKP or SPKM can be used in a single-ended application. The output can drive a 300 Ω load.

Table 2-2. RCSCP2 Pin Signal Definitions (Continued)

Label	I/O Type	Signal/Definition
LINEIN	I(DA)	**Line In Analog Input.** LINEIN is a single-ended input from the audio interface circuit for routing from the handset through the hybrid circuit.
LINEOUT	O(DF)	**Line Out Analog Output.** LINEOUT is a single-ended output to the audio interface circuit for routing to the handset through the hybrid circuit. The output can drive a 600 Ω load.
GENERAL PURPOSE INPUT/OUTPUT LINES		
GPI0-GPI7	ID	**General Purpose Inputs.** Eight general-purpose input (GPI) pins are available to the host for programming via the device interface memory.
GPO1-GPO7	OC	**General Purpose Outputs.** Seven general-purpose output (GPO) pins are available to the host for programming via the device interface memory. SLEEPO# is used by the RCSCP2 to control power down mode for the IA (unless disabled by the host). Connect the SLEEPO# output to the IARESET# input. GPO1-GPO7 are all set to a 1 state by a POR (power-on reset).
AUXILIARY SIGNALS		
EN85#	IA	**Enable 85 Bus.** The EN85# input selects the microprocessor bus compatibility. When EN85# is low, the device can interface directly to an 8085 compatible microprocessor bus using READ# and WRITE#. When EN85# is high, the device can interface directly to a 6500 compatible microprocessor.
XCLK	OB	**XCLK Output.** XCLK is a 35.328 MHz clock.
YCLK	IA/OA	**YCLK.** YCLK is a test input for the R6766-21.
REFERENCE SIGNALS		
VREF	REF	**High Voltage Reference.** Connect to VC through 10 µF (polarized, + terminal to VREF) and 0.1 µF (ceramic) in parallel.
VC	REF	**Low Voltage Reference.** Connect to analog ground through 10 µF (polarized, + terminal to VC) and 0.1 µF (ceramic) in parallel.
RBIAS	REF	**Reference Bias.** Connect to analog ground through 120 kΩ.
MICBIAS	REF	**Microphone Bias.** 2.2VDC, 1 mA microphone bias voltage source.
REFCNTL	REF	**Reference Control.** Connect to analog ground.
PLLVDD	PLL	**PLLVDD Connection.** Connect to AGND through 0.1 µF and to VAA through a 0-ohm resistor.
PLLGND	PLL	**PLLGND Connection.** Connect to AGND.
DEVICE INTERCONNECT AND MISCELLANEOUS		
SR1IO	DI	Connect to RCSCP2: CTRLSIN.
CTRLSIN	DI	Connect to RCSCP2: SR1IO.
SR3IN	DI	Connect to RCSCP2: SOUT.
SOUT	DI	Connect to RCSCP2: SR3IN.
SR4OUT	DI	Connect to RCSCP2: SIN.
SIN	DI	Connect to RCSCP2: SR4OUT.
IACLK	DI	Connect to RCSCP2: MCLK.
MCLK	DI	Connect to RCSCP2: IACLK.
IA1CLK	DI	Connect to RCSCP2: ICLK
ICLK	DI	Connect to RCSCP2: IA1CLK.
SA1CLK	DI	Connect to RCSCP2: FSYNC.
FSYNC	DI	Connect to RCSCP2: SA1CLK.

Notes:

DI = Device interconnect.	MI = Modem interconnect
IA, IB, IC, ID = Digital input (see Table 2-3).	I = Analog input
OA, OB, OC = Digital output (see Table 2-3).	O = Analog output
I(DA) = Analog input (see Table 2-4).	PWR = Power
O(DD), O(DF) = Analog output (see Table 2-4).	GND = Ground

Table 2-3. Digital Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input High Voltage	V_{IH}				VDC	
Type IA		2.0	–	5.25		
Type IB		0.7 V_{DD}	–	5.25		
Input High Current	I_{IH}				µA	V_{DD} = 3.6V, V_{IN}= 3.6 V
Type IA		–	–	40		
Type IB		–	–	40		
Input Low Voltage	V_{IL}				VDC	
Type IA		0	–	0.8		
Type IB		0	–	0.8		
Input Low Current	I_{IL}				µA	V_{DD} = 3.6 V
Type IA and IB		–	–	–400		
Input Leakage Current	I_{IN}		–		µADC	
Types IA and IB				±2.5		
Output High Voltage	V_{OH}		–	–	VDC	
Type OA, OB		2.4	–	–		I_{LOAD} = 2 ma
Type OC		2.4	–	–		I_{LOAD} = 4 ma
Output Low Voltage	V_{OL}				VDC	
Type OA, OB		–	–	0.4		I_{LOAD} = -2 ma
Type OC		–	–	0.4		I_{LOAD} = 4 ma
Output Leakage Current	I_{LO}			±10	µADC	
Types OA and OB						
Capacitive Load	C_L				pF	
Types IA, IB			–	10		
Capacitive Drive	C_D				pF	
Types OA, OB, and OC			–	10		
Circuit Type						
Type IA						TTL
Type IB						Schmitt trigger input
Types OA and OB						TTL
Type OC						TTL with 3-state

Note:

1. Test Conditions: VDD =±5%, TA = 0 C to 70 C, (unless otherwise stated)
   Output Load Conditions: Data bus (D0-D7), address bus (RS0-RS4), chip selects, READ#, and WRITE# loads = 70 pF + one TTL load. Other = 50 pF + one TTL load.

Table 2-4. Analog Electrical Characteristics

Name	Type	Characteristic	Value
LINEIN	I (DA)	Input Impedance AC Input Voltage Range Reference Voltage*	> 38K Ω 2.0 VP-P Single-ended +2.5 VDC
LINEOUT	O (DD)	Minimum Load Maximum Capacitive Load Output Impedance AC Output Voltage Range Reference Voltage* DC Offset Voltage	350 Ω 0.12 µF 10 Ω 2.2 VP-P Single-ended +2.5 VDC ± 200 mV
SPKP and SPKM	O (DF)	Minimum Load Maximum Capacitive Load Output Impedance AC Output Voltage Range Reference Voltage* DC Offset Voltage	300 Ω 0.1 µF 10 Ω 4.0 VP-P Differential +2.5 VDC ± 20 mV
MICIN	I (DA)	Input Impedance Maximum AC Input Voltage Reference Voltage*	> 38K Ω 2.0 VP-P Single-ended +2.5 VDC
* Reference Voltage provided internal to the device.			

Table 2-5. Current and Power Requirements

Mode	Supply	Current		Power		
		Typical Current (mA)	Maximum Current (mA)	Typical Power (mW)	Minimum Power (mW)	Maximum Power (mW)
Normal	3.3V	77.6	88.9	256	210	320
	5.0V	TBD	TBD	TBD	TBD	TBD
Sleep	3.3V	6.7	11.7	22	18	42
	5.0V	TBD	TBD	TBD	TBD	TBD
Notes: Test conditions: VDD = 3.3VDC for typical, VDD = 3.0VDC for minimum, 3.6VDC for maximum						

Table 2-6. Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage	V_{DD}	-0.5 to +3.6	V
Input Voltage	V_{IN}	-0.5 to (+5VD +0.5)	V
Analog Inputs	V_{IN}	-0.3 to (+5VA + 0.3)	V
Voltage Applied to Outputs in High Impedance (Off) State	V_{HZ}	-0.5 to (+5VD + 0.5)	V
DC Input Clamp Current	I_{IK}	±20	ma
DC Output Clamp Current	I_{OK}	±20	ma
Static Discharge Voltage (25°C)	V_{ESD}	±2500	V
Latch-up Current (25°C)	I_{TRIG}	±200	ma
Operating Temperature Range	T_A		°C
Commercial		0 to +70	
Extended		-40 to +85	
Storage Temperature Range	T_{STG}	-55 to +125	°C
ESD Bus Voltage	V_{GG}	-0.5 to (+5VD +0.5)	V

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3. INTERFACE MEMORY

The RCSCP2 communicates with the host processor by means of a dual-port, interface memory. The interface memory in the RCSCP2 contains thirty-two 8-bit registers, labeled register 00 through 1F (Figure 3-1). Each register can be read from, or written into, by both the host and the RCSCP2. The host can control RCSCP2 operation by writing control bits to RCSCP2 interface memory and writing parameter values to RCSCP2 RAM through interface memory. The host can monitor RCSCP2 operation by reading status bits from RCSCP2 interface memory and reading parameter values from RCSCP2 RAM through interface memory.

The interface memory bits and data are illustrated in the register map shown in Figure 3-1.

Table 3-1 lists the interface memory bits and data by major using function.

The Interface memory bits and data are defined in Table 3-2. The interface memory bits are referred to using the format Z:Q. The register number is designated by Z (00 through 1F), and the bit number by Q (0 through 7, 0 = least significant bit).

Register Function	Reg. Addr.	Bit 7	6	5	4	3	2	1	0	Default
Interrupt Handling	1F	PIA	—	—	PIE	PIREQ	—	—	NEWC	-XX0-XX0
	1E	R10IA	R00IA	R10IE	—	R10A	R00IE	—	R00A	--0X-0X-
FDSP Control	1D	FDXEN	AECDIS	HDSET	—	AGCMIC	—	—	SPKLVL1	000X1XX0
	1C	SPKLVL0	VOLUP	VOLDWN	SP/HS	MUTESPK	MUTEMIC	MICLVL1	MICLVL0	00000001
Reserved	1B	—	—	—	—	—	—	—	—	XXXXXXXX
	1A	—	—	—	—	—	—	—	—	--0X-0X-
	19	—	—	—	—	—	—	—	—	XXX000XX
	18	—	—	—	—	—	—	—	—	X00000X0
	17	—	—	—	—	—	—	—	—	XXXXXXXX
	16	—	—	—	—	—	—	—	—	XXXXXXXX
	15	—	—	—	—	—	—	—	—	XXXXXXXX
	14	—	—	—	—	—	—	—	—	XXXXXXXX
Coder Buffer	13	Coder Buffer 1 (CDB1)								--------
	12	Coder Buffer 2 (CDB2								--------
	11	Coder Buffer 3 (CDB3)								--------
	10	Coder Buffer 4 (CDB4)								--------
GPO Control	0F	GPO7	GPO6	GPO5	GPO4	—	—	—	—	0000XXXX
Reserved	0E	—	—	—	—	—	—	—	—	XXXXXXXX
Tone Transmit Control/ Speech Codec Control	0D	—	—	—	—	DTTX/ SIDVDCD	NTDCD	HIOE	—	XXXX000X
Speech Codec Control	0C	APFEN	FRMERA	DCDEN	CDEN	VOXENC/E NCR64	DCRMEN	—	VADEN	10000000
Speech Codec Status	0B	—	—	—	—	VOX	—	—	DCDRDY	XXXX0XX0
	0A	—	—	—	—	—	—	SIDVENC	NTENC	XXXXXX00
Programmable Interrupt	09	ITBMSK								00000000
	08	TRIG		ANDOR	ITADRS					00000000
Speech Codec Control	07	—	—	—	—	—	—	—	—	0XXXXXXX
Configuration	06	CONF**								10010000
RAM Access Control	05	ACC	—	—	—	IO	—	WRT	CR	1XXX0X01
RAM Access Address & Data/ Decoder Buffer	04	RAM ADDRESS (ADD)								00001010
	03	X RAM DATA MSB (XDAM)/Decoder Buffer 1 (DCDB1)								--------
	02	X RAM DATA LSB (XDAL)/Decoder Buffer 2 (DCDB2)								--------
	01	Y RAM DATA MSB (YDAM)/Decoder Buffer 3 (DCDB3)								--------
	00	Y RAM DATA LSB (YDAL)/Decoder Buffer 4 (DCDB4)								--------

Notes:

** A changed value in this register requires the setting of NEWC to become active.

— This symbol in the "Bit" columns indicates that the bit is reserved (do not alter X value in "Default Value" column).

The - symbol in the "Default Value" column indicates that the value is determined by operating conditions.

The Default value reflects power-on reset value.

Figure 3-1. Interface Memory Map

Table 3-1. Interface Memory Bits by Function

General			RAM Access			Interrupt Handling		
Control	Status	Data	Control	Status	Data	Control	Status	Data
CONF			ACC	R00A	XDAL	R00IE	R00A	
NEWC			ADD	R00IA	XDAM	R10IE	R00IA	
			CR		YDAL		R10A	
			IO		YDAM		R10IA	
			WRT					

Programmable Interrupt			General Purpose Input/Output			Dual Tone Transmit		
Control	Status	Data	Control	Status	Data	Control	Status	Data
PIE	PIA		GPO4			DTTX		
PIREQ			GPO5					
ITBMSK			GPO6					
ANDOR			GPO7					
ITADRS								
TRIG								

G.711-Handset/Headset			G.711-HDSP			G.711-FDSP		
Control	Status	Data	Control	Status	Data	Control	Status	Data
CDEN		CDB1	AGCMIC		CDB1	AGCMIC		CDB1
DCDEN		CDB2	MICLVL0		CDB2	MICLVL0		CDB2
SP/HS		CDB3	MICLVL1		CDB3	MICLVL1		CDB3
		CDB4	MUTEMIC		CDB4	MUTEMIC		CDB4
		DCDB1	MUTESPK		DCDB1	MUTESPK		DCDB1
		DCDB2	SP/HS		DCDB2	SP/HS		DCDB2
		DCDB3	VOLDWN		DCDB3	FDXEN		DCDB3
		DCDB4	VOLUP		DCDB4	HDSET		DCDB4
			CDEN			VOLDWN		
			DCDEN			VOLUP		
						CDEN		
						DCDEN		

G.728-Handset/Headset			G.728-HDSP			G.728-FDSP		
Control	Status	Data	Control	Status	Data	Control	Status	Data
CDEN		CDB1	AGCMIC		CDB1	AGCMIC		CDB1
DCDEN		CDB2	MICLVL0		CDB2	MICLVL0		CDB2
SP/HS		CDB3	MICLVL1		CDB3	MICLVL1		CDB3
		CDB4	MUTEMIC		CDB4	MUTEMIC		CDB4
		DCDB1	MUTESPK		DCDB1	MUTESPK		DCDB1
		DCDB2	SP/HS		DCDB2	SP/HS		DCDB2
		DCDB3	VOLDWN		DCDB3	FDXEN		DCDB3
		DCDB4	VOLUP		DCDB4	HDSET		DCDB4
			CDEN			VOLDWN		
			DCDEN			VOLUP		
						CDEN		
						DCDEN		

Table 3-1. Interface Memory Bits by Function (Continued)

G.729-Handset/Headset			G.729-HDSP			G.729-FDSP		
Control	**Status**	**Data**	**Control**	**Status**	**Data**	**Control**	**Status**	**Data**
APFEN	NTENC	CDB1	AGCMIC	NTENC	CDB1	AGCMIC	NTENC	CDB1
CDEN	SIDVENC	CDB2	MICLVL0	SIDVENC	CDB2	MICLVL0	SIDVENC	CDB2
DCDEN		CDB3	MICLVL1		CDB3	MICLVL1		CDB3
FRMERA		CDB4	MUTEMIC		CDB4	MUTEMIC		CDB4
SP/HS		DCDB1	MUTESPK		DCDB1	MUTESPK		DCDB1
NTDCD		DCDB2	SP/HS		DCDB2	SP/HS		DCDB2
SIDVDCD		DCDB3	FDXEN		DCDB3	FDXEN		DCDB3
VADEN		DCDB4	VOLDWN		DCDB4	HDSET		DCDB4
			VOLUP			VOLDWN		
			APFEN			VOLUP		
			CDEN			APFEN		
			DCDEN			CDEN		
			FRMERA			DCDEN		
			NTDCD			FRMERA		
			SIDVDCD			NTDCD		
			VADEN			SIDVDCD		
						VADEN		

G.723.1-Handset/Headset			G.723.1-HDSP			G.723.1-FDSP		
Control	**Status**	**Data**	**Control**	**Status**	**Data**	**Control**	**Status**	**Data**
APFEN	NTENC	CDB1	AGCMIC	NTENC	CDB1	AGCMIC	NTENC	CDB1
CDEN		CDB2	MICLVL0		CDB2	MICLVL0		CDB2
DCDEN		CDB3	MICLVL1		CDB3	MICLVL1		CDB3
FRMERA		CDB4	MUTEMIC		CDB4	MUTEMIC		CDB4
SP/HS		DCDB1	MUTESPK		DCDB1	MUTESPK		DCDB1
DCRMEN		DCDB2	SP/HS		DCDB2	SP/HS		DCDB2
ENCR64		DCDB3	VOLDWN		DCDB3	FDXEN		DCDB3
NTDCD		DCDB4	VOLUP		DCDB4	HDSET		DCDB4
VADEN			APFEN			VOLDWN		
			CDEN			VOLUP		
			DCDEN			APFEN		
			FRMERA			CDEN		
			DCRMEN			DCDEN		
			ENCR64			FRMERA		
			NTDCD			DCRMEN		
			VADEN			ENCR64		
						NTDCD		
						VADEN		

Table 3-1. Interface Memory Bits by Function (Continued)

DigiTalk-Handset/Headset			DigiTalk-HDSP			DigiTalk -FDSP		
Control	**Status**	**Data**	**Control**	**Status**	**Data**	**Control**	**Status**	**Data**
APFEN	VOX	CDB1	AGCMIC	VOX	CDB1	AGCMIC	VOX	CDB1
CDEN		CDB2	MICLVL0		CDB2	MICLVL0		CDB2
DCDEN		CDB3	MICLVL1		CDB3	MICLVL1		CDB3
FRMERA		CDB4	MUTEMIC		CDB4	MUTEMIC		CDB4
SP/HS		DCDB1	MUTESPK		DCDB1	MUTESPK		DCDB1
VOXENC		DCDB2	SP/HS		DCDB2	SP/HS		DCDB2
		DCDB3	VOLDWN		DCDB3	FDXEN		DCDB3
		DCDB4	VOLUP		DCDB4	HDSET		DCDB4
			VOXENC			VOLDWN		
			APFEN			VOLUP		
			CDEN			VOXENC		
			DCDEN			APFEN		
			FRMERA			CDEN		
						DCDEN		
						FRMERA		

Table 3-2. Interface Memory Bit Definitions

Mnemonic	Location	Default	Name/Description
ACC	05:7	1	**RAM Access.** When control bit ACC is a 1, the RCSCP2 accesses the RAM associated with the address in ADD and the CR bit. WRT determines if a read or write is performed.
ADD	04:0-7	0A	**RAM Address.** ADD contains the RAM address used to access the RCSCP2's X and Y Data RAM (CR = 0) or X and Y Coefficient RAM (CR = 1) via the X RAM Data least significant byte (LSB) and most significant byte (MSB) words (02:0-7 and 03:0-7, respectively) and the Y RAM Data LSB and MSB words (00:0-7 and 01:0-7, respectively).
AECDIS	1D:6	0	**AEC Disable.** Control bit AECDIS disables (AECDIS = 1) or enables (AECDIS = 0) the acoustic echo canceller (FDSP mode).
AGCMIC	1D:3	1	**Microphone AGC.** Control bit AGCMIC enables (AGCMIC = 1) or disables (AGCMIC = 0) the microphone digital automatic gain control (FDSP mode).
ANDOR	08:5	0	**AND/OR Bit Mask Function.** When control bit ANDOR is set and the programmable interrupt is enabled (PIE is set), the RCSCP2 will assert ~IRQ if all the bits in the register specified by ITADRS and masked by ITBMSK are set. When ANDOR is reset and the programmable interrupt is enabled, the RCSCP2 will assert ~IRQ if any one of the bits in the register specified by ITADRS and masked by ITBMSK is set.
APFEN	0C:7	1	**Adaptive Postfilter Enable.** The APFEN control bit enables (APFEN = 1) or disables (APFEN = 0) the Decoder adaptive postfilter.
CDB1	13:0-7	-	**Coder Data Buffer 1.** Coder Data Buffer 1 to be read by the host when status bit R10A is set by the RCSCP2 when the RCSCP2 is writing to CDB4.
CDB2	12:0-7	-	**Coder Data Buffer 2.** Coder Data Buffer 2 to be read by the host when status bit R10A is set by the RCSCP2 when the RCSCP2 is writing to CDB4.
CDB3	11:0-7	-	**Coder Data Buffer 3.** Coder Data Buffer 3 to be read by the host when status bit R10A is set by the RCSCP2 when the RCSCP2 is writing to CDB4.
CDB4	10:0-7	-	**Coder Data Buffer 4.** Coder Data Buffer 4 to be read last by the host when status bit R10A is set by the RCSCP2 when the RCSCP2 is writing to CDB4.
CDEN	0C:4	0	**Coder Enable.** When control bit CDEN is set, the RCSCP2 performs coding. The coder output is placed into buffers CDB1, CDB2, CDB3, and CDB4. The RCSCP2 writing to CDB4 sets R10A.
CONF	06:0-7	90	**Configuration.** The CONF control bits select one of the following configurations: **CONF (Hex) Configuration** D4 G.711 Codec (A-Law) (See Note 1.) D0 G.711 Codec (μ-Law) (See Note 1.) B0 G.723.1 and G.723.1 Annex A Codec (See Notes 1 and 2.) 98 G.729 and G.729 Annex B Codec (See Notes 1 and 2.) 92 G.728 Codec (See Note 1.) 90 DigiTalk Codec (See Note 1.) 80 Dual Tone Transmit: Transmit Tones: DTTX on: Squelch: DTTX off: Notes: 1. Handset, Headset Mode, or FDSP mode selection: Handset Mode: SP/HS off, FDXEN dc, HDSET dc, HECDIS off Headset Mode: SP/HS on, FDXEN on, HDSET on, HECDIS dc FDSP Mode: SP/HS on, FDXEN on, HDSET off, HECDIS dc dc = Don't care. 2. Voice Activity Detector enabled/disabled: Voice Activity Detector Disabled: VADEN off Voice Activity Detector Enabled: VADEN on

Table 3-2. Interface Memory Bit Definitions (Continued)

Mnemonic	Location	Default	Name/Description
CR	05:0	1	**Coefficient RAM Select.** When control bit CR is a 1, ADD addresses Coefficient RAM. When CR is a 0, ADD addresses Data RAM. This bit must be set according to the desired RAM address (Table 4-1).
DCDB1	03:0-7	-	**Decoder Data Buffer 1.** Decoder Data Buffer 1 to be written by the host when status bit R00A is set by the RCSCP2 when the RCSCP2 is reading from DCDB4.
DCDB2	02:0-7	-	**Decoder Data Buffer 2.** Decoder Data Buffer 2 to be written by the host when status bit R00A is set by the RCSCP2 when the RCSCP2 is reading from DCDB4.
DCDB3	01:0-7	-	**Decoder Data Buffer 3.** Decoder Data Buffer 3 to be written by the host when status bit R00A is set by the RCSCP2 when the RCSCP2 is reading from DCDB4.
DCDB4	00:0-7	-	**Decoder Data Buffer 4.** Decoder Data Buffer 4 to be written last by the host when status bit R00A is set by the RCSCP2 when the RCSCP2 is reading from DCDB4.
DCDEN	0C:5	0	**Decoder Enable.** When control bit DCDEN is set, the RCSCP2 performs decoding. The Decoder input is placed into buffers DCDB1, DCDB2, DCDB3, and DCDB4. The RCSCP2 reading data buffer DCDB4 sets R00A.
DCRMEN	0C:2	-	**Encoder DC Remover Enable**. When DCRMEN control bit is set, the DC remover compliant to G.723.1 is enabled. (G.723.1)
DCDRDY	0B:0	0	**Decoder Ready.** When control bit HIOE (0D:1) is set and the Decoder is enabled (DCDEN = 1), status bit DCDRDY is set by the RCSCP2 when the Decoder is ready for the host to transfer the next frame of coded speech to the RCSCP2.
DTTX	0D:3	0	**Dual Tone Transmit Enable.** The DTTX control bit enables (DTTX = 1) or disables (DTTX = 0) dual tone transmission. (Dual Tone Transmit)
ENCR64	0C:3	-	**Encoder High Rate Control**. When CDEN and ENCR64 control bits are set, the Coder will operate in high rate mode. When CDEN is set and ENCR64 reset, the Coder will operate in low rate mode. This bit may be changed while the Coder is enabled. (G.723.1)
FDXEN	1D:1	0	**Full-Duplex Speakerphone Enable.** Control bit FDXEN enables (FDXEN = 1) or disables (FDXEN = 0) full-duplex speakerphone operation. FDXEN must be set before setting SP/HS (FDSP mode).
FRMERA	0C:6	0	**Frame Erasure.** When the host receives a corrupted frame of coded speech data, the host informs the Decoder of a frame erasure by setting control bit FRMERA. The host must reset FRMERA whenever the received frame of coded speech data is not corrupted.
GPOx	0F:4-7	0	**General Purpose Outputs.** Bits 4-7 in the GPOx register, set/reset by the host, are reflected by logic level outputs (1 = high, 0 = low) appearing on signals GPO4-GPO7, respectively, within 125 microseconds of bit transition.
HDSET	1D:5	0	**Headset Mode.** Control bit HDSET enables (HDSET = 1) or disables (HDSET = 0) headset operation. During headset operation, the speakerphone acoustic echo canceller and automatic loop-gain controls are disabled (FDSP mode).
HIOE	0D:1	0	**Host Input/Output Enable.** The host sets control bit HIOE when the Coder input is to be read from interface memory registers or the Decoder output is to be written to the interface memory registers.
IO	05:3	0	**Input/Output RAM Select.** When control bit IO is a 1, ADD addresses IO RAM. When IO is a 0, ADD addresses either coefficient or data RAM depending on the state of the CR bit. This bit must be set according to the desired RAM address (Table 4-1).

Table 3-2. Interface Memory Bit Definitions (Continued)

Mnemonic	Location	Default	Name/Description
ITADRS	08:0-4	0	**Interrupt Address.** These five bits specify the register upon which the programmable interrupt and ITBMSK will affect. The address of the byte on which the RCSCP2 asserts ~IRQ on a bit or bits in that byte is: **Host Register (Hex) / ITADRS (Hex) / Host Register (Hex) / ITADRS (Hex)** 00 / 00 / 10 / 08 01 / 10 / 11 / 18 02 / 01 / 12 / 09 03 / 11 / 13 / 19 04 / 02 / 14 / 0A 05 / 12 / 15 / 1A 06 / 03 / 16 / 0B 07 / 13 / 17 / 1B 08 / 04 / 18 / 0C 09 / 14 / 19 / 1C 0A / 05 / 1A / 0D 0B / 15 / 1B / 1D 0C / 06 / 1C / 0E 0D / 16 / 1D / 1E 0E / 07 / 1E / 0F 0F / 17 / 1F / 1F
ITBMSK	09:0-7	00	**Interrupt Bit Mask.** This byte performs a bit mask on the register specified in ITADRS for the programmable interrupt processing. A one in any position in ITBMSK will cause the RCSCP2 to assert ~IRQ on the corresponding bit or bits in the register specified by ITADRS according to the ANDOR bit and the TRIG bits if PIE is set and PIREQ reset by the host.
MICLVL	1C:0-1	01	**Microphone Gain.** These two bits control the microphone input analog gain as follows (FDSP mode): **MICLVL1 / MICLVL0 / Gain** 0 / 0 / 0 dB 0 / 1 / 10 dB 1 / 0 / 15 dB 1 / 1 / 20 dB
MUTEMIC	1C:2	0	**Mute Microphone Input.** Control bit MUTEMIC enables (MUTEMIC = 1) or disables (MUTEMIC = 0) muting of the microphone input signal. (FDSP Mode)
MUTESPK	1C:3	0	**Mute Speaker Output.** Control bit MUTESPK enables (MUTESPK = 1) or disables (MUTESPK = 0) muting of the speaker output signal. (FDSP Mode)
NEWC	1F:0	0	**New Configuration.** The host must set control bit NEWC after the host writes a configuration code into the CONF bits (register 6:0-7). Setting the NEWC bit informs the RCSCP2 to implement the configuration change. The RCSCP2 resets the NEWC bit when the configuration change request is recognized.
NTDCD	0D:2	-	**Decoder Frame NT Control**. NTDCD control bit is set by the host when the current received speech frame is a non-transmitted (NT) frame; NTDCD is reset by the host if the current received frame is VOICED or SID frame. (G.729 and G.723.1)
NTENC	0A:0	-	**Coder Frame NT Status**. NTENC status bit is set by the RCSCP2 if current coded frame is a non-transmitted (NT) frame; NTENC is reset by the RCSCP2 if current coded frame is VOICED or SID frame. (G.729 and G.723.1)
PIA	1F:7	-	**Programmable Interrupt Active.** When control bit PIE is enabled (PIE is set) and the interrupt condition is true as specified by ITBMSK, ITADRS, TRIG, and ANDOR, the RCSCP2 asserts ~IRQ if PIREQ has been previously reset by the host. Status bit PIA is set by the RCSCP2 when the above occurs. PIA is reset when the host resets PIREQ.

Table 3-2. Interface Memory Bit Definitions (Continued)

Mnemonic	Location	Default	Name/Description
PIE	1F:4	0	**Programmable Interrupt Enable.** When control bit PIE is enabled (PIE is set) and the interrupt condition is true as specified by ITBMSK, ITADRS, TRIG, and ANDOR, the RCSCP2 asserts ~IRQ if PIREQ has been previously reset by the host. Status bit PIA is set by the RCSCP2 when the above occurs. When PIE is reset, ITBMSK, ITADRS, TRIG, ANDOR, and PIREQ have no effect on ~IRQ and PIA.
PIREQ	1F:3	-	**Programmable Interrupt Request.** When control bit PIE is enabled (PIE is set) and the interrupt condition is true as specified by ITBMSK, ITADRS, TRIG, and ANDOR, the RCSCP2 asserts ~IRQ if control bit PIREQ has been previously reset by the host. PIREQ is set by the RCSCP2 when the programmable interrupt condition is true. The host must reset PIREQ after servicing the interrupt since the RCSCP2 does not reset PIREQ. If PIREQ is not reset when the interrupt condition occurs again, the RCSCP2 will not assert ~IRQ.
R00A	1E:0	-	**Register 00 Available.** When set, status bit R00A signifies that the RCSCP2 has either written diagnostic data to, or read diagnostic data from, Register 00. If the Decoder is enabled (DCDEN = 1), the RCSCP2 sets R00A when the Register 00 has been read by the Decoder. Setting R00A can also cause ~IRQ to be asserted. The host writing to or reading from Register 00 resets the R00A and R00IA bits. (See R00IE and R00IA.)
R00IE	1E:2	0	**Register 00 Interrupt Enable.** When control bit R00IE is set, assertion of ~IRQ is enabled for Register 00, i.e., the RCSCP2 will assert ~IRQ and set R00IA when R00A is set. When R00IE is reset, R00A has no effect on ~IRQ and R00IA. (See R00A and R00IA.)
R00IA	1E:6	-	**Register 00 Interrupt Active.** When Register 00 Interrupt is enabled (R00IE is set) and R00A is set by the RCSCP2, the RCSCP2 asserts ~IRQ and sets status bit R00IA to indicate that R00A caused the interrupt. The host writing to or reading from register 00 resets R00IA. (See R00IE and R00A.)
R10A	1E:3	-	**Register 10 Available.** If the Coder is enabled (CDEN = 1), the RCSCP2 sets R10A when Register 10 has been written by the Coder. Setting R10A can also cause ~IRQ to be asserted. The host writing to or reading from register 10h resets the R10A and R10IA bits to 0. (See R10IE and R10IA.)
R10IE	1E:5	0	**Register 10 Interrupt Enable.** When control bit R10IE is set, assertion of ~IRQ is enabled for Register 10, i.e., the RCSCP2 will assert ~IRQ and set R10IA when R10A is set. When R10IE is reset, R10A has no effect on ~IRQ and R10IA. (See R10A and R10IA.)
R10IA	1E:7	-	**Register 10 Interrupt Active.** When Register 10 Interrupt is enabled (R10IE is set) and R10A is set by the RCSCP2, the RCSCP2 asserts ~IRQ and sets status bit R10IA to indicate that R10A caused the interrupt. The host writing to or reading from register 10 resets R10IA. (See R10IE and R10A.)
SIDVDCD	0D:3	-	**Decoder Frame SID Flag Control**. SIDVDCD control bit is set by the host when the current received speech frame is VOICED; SIDVDCD is reset by the host if the current received speech frame is a SID frame. (G.729)
SIDVENC	0A:1	-	**Encoder Frame SID Flag Status**. SIDVENC status bit is set by the RCSCP2 if current coded frame is a VOICED frame; SIDVENC is reset by the RCSCP2 if current coded frame is a SID frame. (G.729)
SP/HS	1C:4	0	**Speakerphone/Handset Select.** When SP/HS is a 1, speakerphone operation is selected. When SP/HS is a 0, handset operation is selected.
SPKLVL0 SPKLVL1	1C:1 1D:0	0 0	**Speaker Gain.** These two bits control the speaker digital gain as follows (FDSP mode): **SPKLVL1 SPKPLVL0 Gain** 0 0 0 dB 0 1 6 dB 1 0 9.5 dB 1 1 12 dB

Table 3-2. Interface Memory Bit Definitions (Continued)

Mnemonic	Location	Default	Name/Description
TRIG	08:6-7	0	**Interrupt Triggering.** These two bits select how the programmable interrupt is to occur if this interrupt is enabled (PIE = 1). The host has the option to be continuously interrupted whenever the interrupt condition is true (DC triggered), to be interrupted only when the interrupt condition transitions from false to true (positive edge triggered), to be interrupted only when the interrupt condition transitions from true to false (negative edge triggered), or to be interrupted when the interrupt condition transitions from false to true and when the mode transitions from true to false (edge triggered): **Bit 7** **Bit 6** **Description** 0 0 DC Level Triggered 0 1 Positive Edge Triggered 1 0 Negative Edge Triggered 1 1 Edge Triggered
VADEN	0C:0	-	**VAD Enable**. When CDEN and VADEN control bits are set, the voice activity detector is enabled for G.729 Annex B or G.723.1 Annex A. When VADEN is reset, the voice activity detector is disabled. (G.729 and G.723.1)
VOLDWN	1C:5	0	**Volume Down.** The speaker volume is decreased by 1 dB each time the VOLDWN bit is set. The VOLDWN bit is automatically reset by the RCSCP2. (FDSP Mode.)
VOLUP	1C:6	0	**Volume Up.** The speaker volume is increased by 1 dB each time control bit VOLUP is set. The VOLUP bit is automatically reset by the RCSCP2. (FDSP Mode.)
VOX	0B:3	0	**Voice Detect.** Status bit VOX is set when the Coder is detecting speech and is reset when the Coder is not detecting speech. (DigiTalk.)
VOXENC	0C:3	0	**Voice Activated Encoding.** When control bits VOXENC and CDEN are set, speech coding is delayed until speech is detected and status bit VOX is set. When VOXENC is reset, speech coding is not delayed. (DigiTalk.)
WRT	05:1	0	**RAM Write.** When control bit WRT is a 1 and ACC is a 1, the RCSCP2 writes the data from the Y RAM Data registers into its internal RAM at the location addressed by ADD and CR. (When the most significant bit of ADD is a 0, the write is performed to the X RAM location; when a 1, the write is to the Y RAM location.) When WRT is a 0 and ACC is set to a 1, the RCSCP2 reads data from its internal RAM from the locations addressed by ADD and CR, and stores the data into the X RAM Data registers and Y RAM Data registers, respectively.
XDAL	02:0-7	–	**X RAM Data LSB.** XDAL is the LSB of the 16-bit X RAM data word used in reading X RAM locations.
XDAM	03:0-7	–	**X RAM Data MSB.** XDAM is the MSB of the 16-bit X RAM data word used in reading X RAM locations.
YDAL	00:0-7	–	**Y RAM Data LSB.** YDAL is the LSB of the 16-bit Y RAM data word used in reading Y RAM locations, or writing X or Y RAM locations.
YDAM	01:0-7	–	**Y RAM Data MSB.** YDAM is the MSB of the 16-bit Y RAM data word used in reading Y RAM locations, or writing X or Y RAM locations.

4. RAM PARAMETER ACCESS AND SCALING

4.1 RCSCP2 RAM ACCESS

The RCSCP2 contains 16-bit words of random access memory (RAM).

The RAM is organized into X RAM and Y RAM parts. The host processor can read or write both the X RAM and the Y RAM.

RCSCP2 interface memory is an intermediary during data exchanges between the host and RCSCP2 RAM. The address stored in interface memory RAM address register by the host determines the RCSCP2 RAM address for data access.

The 16-bit words are transferred between RCSCP2 RAM and RCSCP2 interface memory once each sample time. The sample rate is 8000 Hz.

The RCSCP2 main RAM has four RAM banks: Data X RAM, Data Y RAM, Coefficient X RAM, and Coefficient Y RAM.

RAM access is controlled by the ADD, CR, IO, WRT, and ACC bits in RCSCP2 interface memory. The RAM address is specified by the RAM Address bits (ADD). Coefficient RAM or Data RAM access is selected by the Coefficient RAM Select bit (CR). Read or write is selected by the Write bit (WRT). The transfer is initiated by the host setting the RAM Access bit (ACC).

The RCSCP2 RAM access functions, codes, and registers are identified in Table 4-1.

Table 4-1. RAM Parameters and Access Codes

No. [1]	Function	CR	IO	ADD	Read Reg. No.
1	Sleep Mode	0	1	3E	0,1
2	LINEOUT and SPKP/SPKM Attenuation	0	0	05	2,3
3	LINEIN and MICIN Signal Sample	1	0	8A	0,1
4	DigiTalk Noise Energy Level Threshold	0	0	84	0,1
5	Coder Output Delay	0	0	86	0,1
6	DigiTalk VOX Turn-On Threshold	1	0	05	2,3
7	DigiTalk VOX Turn-Off Threshold	1	0	85	0,1
8	DigiTalk VOX A0 Filter Coefficient	1	0	84	0,1
9	DigiTalk VOX A1 Filter Coefficient	1	0	04	2,3
10	Tone 1 Frequency	1	0	06	2,3
11	Tone 2 Frequency	1	0	07	2,3
12	Tone 1 Transmit Output Attenuation	0	0	06	2,3
13	Tone 2 Transmit Output Attenuation	0	0	07	2,3
14	FDSP Microphone AGC Reference Level	1	0	46	2,3
15	FDSP Microphone AGC Slew Rate	1	0	51	2,3
16	FDSP Microphone Speech Hangover	1	0	40	2,3
17	FDSP Speaker Speech Hangover	1	0	C3	0,1

Notes:

1. Parameter numbers refer to corresponding numbers in the following description.

4.1.1 Decoder is Not Enabled

Use the following RAM access procedure when the Decoder is not enabled (DCDEN = 0) (see Figure 4-1).

4.1.1.1 RAM Read Procedure

The RCSCP2 RAM read procedure is a 32-bit transfer from RCSCP2 RAM to the interface memory that transfers both the X RAM and Y RAM simultaneously.

1. Read YDAL to reset R00A.
2. Reset WRT to a 0 to inform the RCSCP2 that a RAM read will occur when ACC is set to a 1.
3. Write the RAM address into ADD.
4. Set CR and IO to the appropriate values.
5. Set ACC to a 1 to signal the RCSCP2 to perform the RAM read.
6. The RCSCP2 sets R00A and resets ACC after transferring the contents of RAM into the interface memory registers.
7. If R00IE is a 1, the RCSCP2 asserts ~IRQ and sets R00IA to a 1 to inform the host that setting of R00A is the cause.
8. When R00A is set, read XDAM, XDAL, YDAM, and YDAL in this order. Note that reading YDAL clears R00IA, which causes ~IRQ to return high if no other interrupt requests are pending.

4.1.1.2 RAM Write Procedure

The RAM write procedure is a 16-bit transfer from interface memory to RCSCP2 RAM allowing the transfer of X RAM data or Y RAM data.

1. Read YDAL to reset R00A.
2. Write the RAM address into ADD.
3. Set CR and IO to the appropriate values.
4. Set WRT to a 1 to inform the RCSCP2 that a RAM write will occur when ACC is set to a 1.
5. Write the parameter MSB to YDAM and the parameter LSB to YDAL.
6. Set ACC to a 1 to signal the RCSCP2 to perform the RAM write.
7. The RCSCP2 sets R00A and resets ACC after transferring the contents of the interface memory registers into RAM.
8. If R00IE is a 1, ~IRQ is also asserted and R00IA is set to a 1 when R00A is set to a 1 by the RCSCP2.
9. Clear R00IA by writing into, or read from, YDAL, which causes ~IRQ to return high if no other interrupt requests are pending.

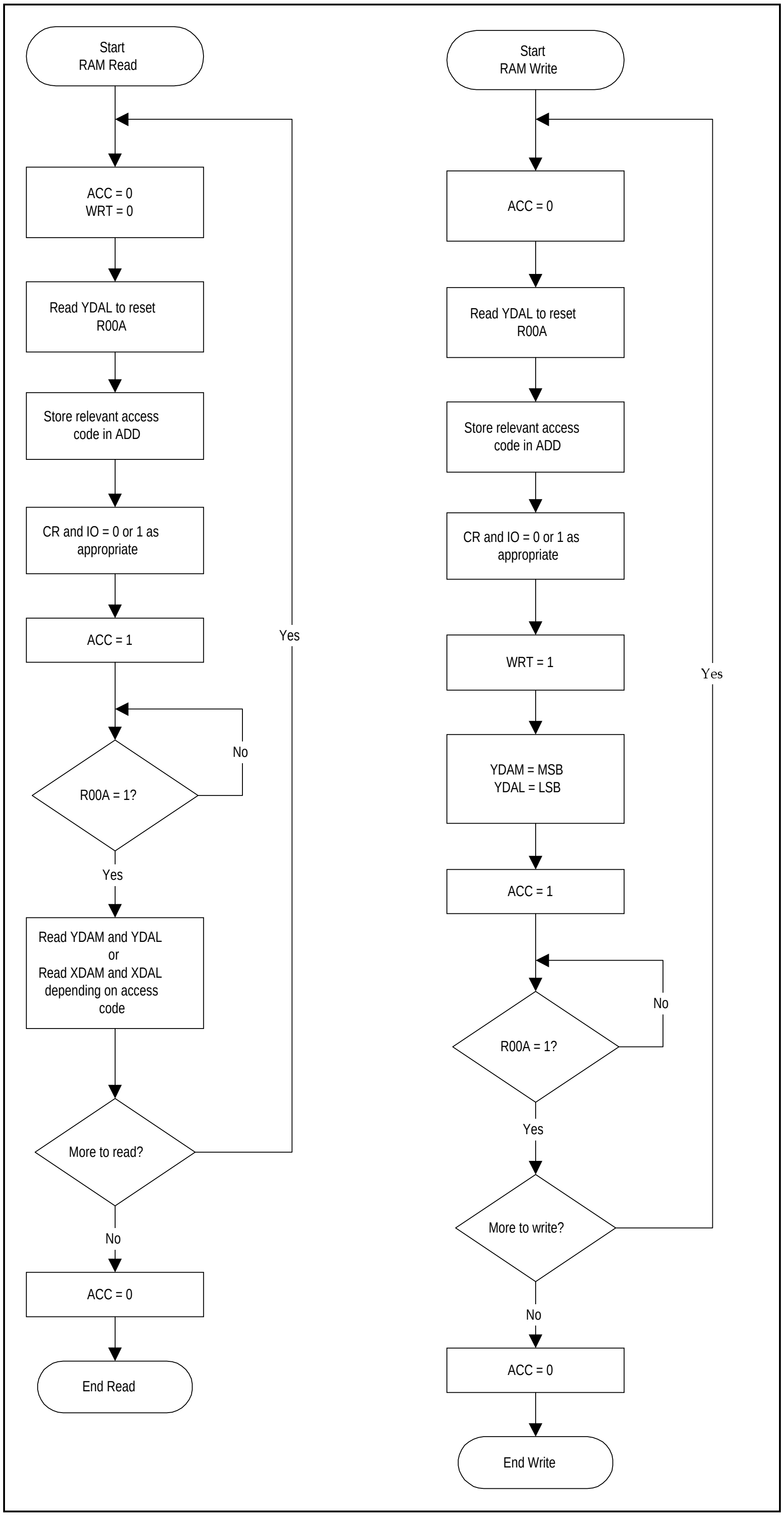

Figure 4-1. Host Flowchart - RAM Access When Decoder is Not Enabled

4.1.2 Decoder is Enabled

Use the following RAM access procedure when the Decoder is enabled (DCDEN = 1) (see Figure 4-2).

4.1.2.1 RAM Read Procedure

The RCSCP2 RAM read procedure is a 32-bit transfer from RCSCP2 RAM to the interface memory that transfers both the X RAM and Y RAM simultaneously.

1. Wait until interrupt active bit (R00A) is set.
2. Set IO to a 1 or a 0 in accordance with the desired parameter IO value.
3. Set CR to a 1 or a 0 in accordance with the desired parameter CR value.
4. Write the RAM address for the desired parameter into ADD.
5. Set WRT to a 0 to inform the RCSCP2 that a RAM read will occur when ACC is set to a 1.
6. Set ACC to a 1 to signal the RCSCP2 to access the RAM.
7. Read or write YDAL to reset R00A.
8. When ACC returns to 0, set ACC to a 1.
9. Read the parameter XDAM, XDAL, YDAL, and YDAL values.
10. Wait until ACC returns to a 0.
11. If more parameters are to be read, go to step 1, otherwise return.

4.1.2.2 RAM Write Procedure

The RAM write procedure is a 16-bit transfer from interface memory to RCSCP2 RAM allowing the transfer of Y RAM data to occur each baud data, or sample time.

1. Wait until interrupt active bit (R00A) is set.
2. Set IO to a 1 or a 0 in accordance with the desired parameter IO value.
3. Set CR to a 1 or a 0 in accordance with the desired parameter CR value.
4. Write the RAM address for the desired parameter into ADD.
5. Set WRT to a 1 to inform the RCSCP2 that a RAM write will occur when ACC is set to a 1.
6. Set ACC to a 1 to signal the RCSCP2 to access the RAM.
7. Write the parameter MSB to YDAM and the parameter LSB to YDAL.
8. Wait until ACC returns to a 0.
9. If more parameters are to be read, go to step 1, otherwise return.

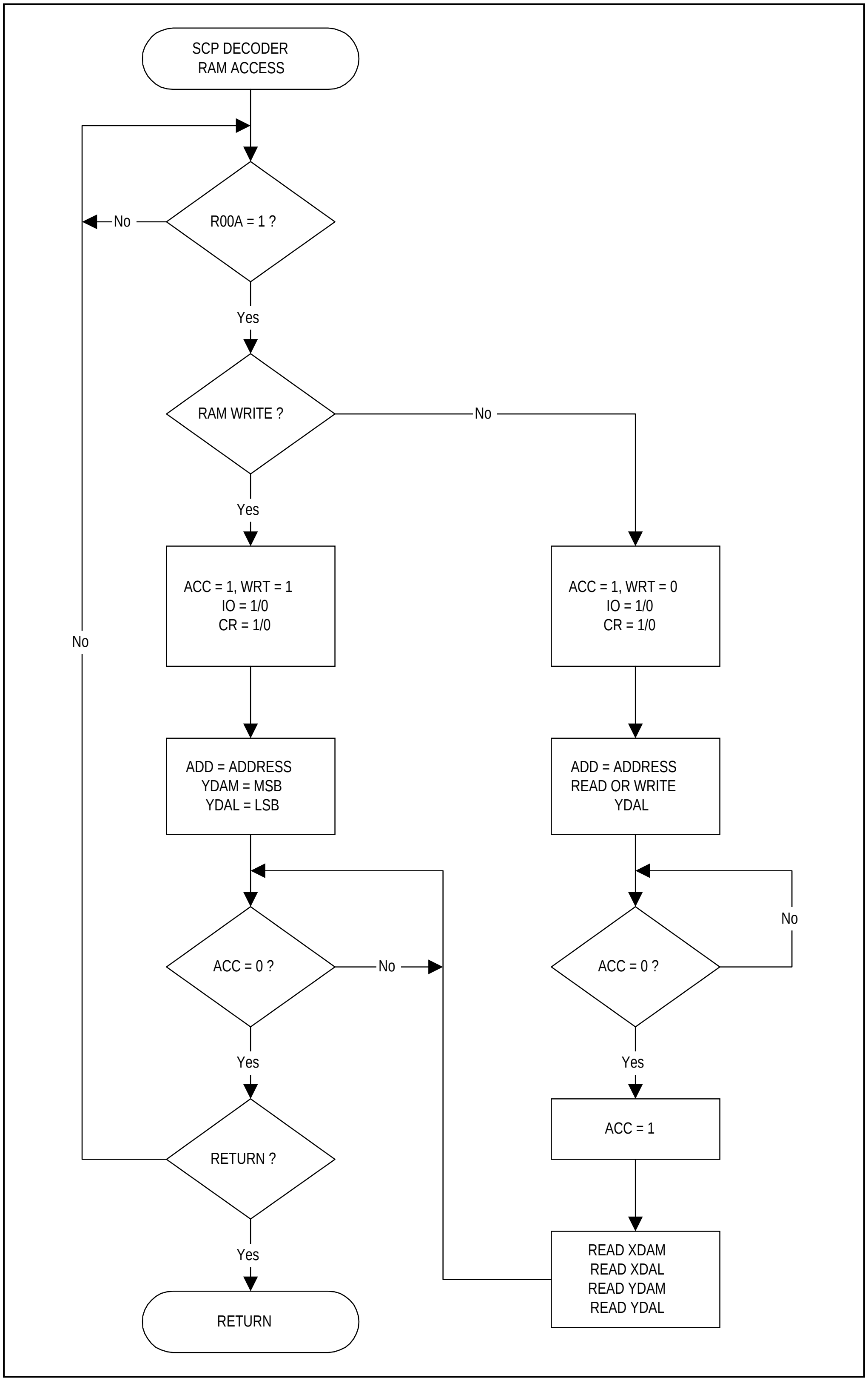

Figure 4-2. Host Flowchart - RAM Access When Decoder is Enabled

4.2 RAM PARAMETER SCALING

1. Sleep Mode

Writing 0 to this register puts the RCSCP2 into the Sleep Mode. The RCSCP2 will go through the power-on sequence and resume normal operation with default values in response to a hardware power-on reset or a write to any interface memory register by the host.

2. LINEOUT and SPKP/SPKM Attenuation

Format: 16-bits, positive, twos complement

Equation: Number = $(10^{[-x/20]})(32767)$

Where: x = dB of attenuation.

Convert Number to hex and store in RAM.

Range: 0 - 7FFFh

Default: 7FFFh

3. LINEIN and MICIN Signal Sample

Format: 16 bits, signed, twos complement

Equation: V_{INT} (Volts)= [(A/D Sample Word x V_{P-P}/65536) + 2.5V (see Table 2-4 for V_{P-P})

Where: V_{EXT} is the input to the IA

V_{INT} is the output of the IA and input to the RCSCP2.

4. DigiTalk Noise Energy Level Threshold

When the remote host detects silence and consequently does not transmit Coder output data across the channel to the local host, the local Decoder inserts comfort noise until the remote host detects speech and resumes Coder data transmission. The inserted comfort noise energy level is set equal to the last received frame's energy provided that this energy is less than or equal to this threshold value. This threshold value can range from 0 (representing silence) to 31 (representing the maximum possible energy output level).

Format: 16-bits, signed, twos complement

Default: 0004h

5. Coder Output Delay

The Coder output data is presented to the host in groups of four or two bytes. The interval between successive groups of bytes of Coder output data may be specified by the host in increments of 125 µs.

Format: 16-bits, signed, twos complement

Equation: Number of 125 microsecond intervals - 1

Default: 0000h (one 125 µs interval)

6. DigiTalk VOX Turn-On Threshold

If status bit VOX (0B:3) is reset, the RCSCP2 sets VOX indicating speech signal detection when the average energy of the speech being coded exceeds the DigiTalk VOX turn-on threshold,.

Format: 16 bits, signed, twos complement

Equation: Level = $(10^{[x/20]})(32767)$

Where: x = VOX turn-on threshold in dB.

Default: 0100h (-42.1 dB)

7. DigiTalk VOX Turn-Off Threshold

If status bit VOX (0B:3) is set, the RCSCP2 resets VOX when the average energy of the speech being coded falls below the DigiTalk VOX turn-off threshold for a minimum period of time equal to the time constant of the VOX energy averaging filter. The time is specified by the VOX energy averaging filter coefficient A0 (see No. 8).

Format: 16 bits, signed, twos complement

Equation: Level = $(10^{[x/20]})(32767)$

Where: x = VOX turn-off threshold in dB.

Default: 0080h (-48.2 dB)

8. DigiTalk VOX A0 Filter Coefficient

VOX energy averaging filter coefficient A0 is a function of the filter time constant.

Format: 16 bits, signed, twos complement

Equation: A0 = 852/x

Where: x = VOX turn-off time in seconds.

Default: 0750h (0.455 seconds)

9. DigiTalk VOX A1 Filter Coefficient

VOX energy averaging filter coefficient A1 is a function of the filter coefficient A0.

Format: 16 bits, signed, twos complement

Equation: A1 = 7FFFh - A0

Where: A0 = VOX energy averaging filter coefficient.

Default: 78AFh

10. Tone 1 Frequency

11. Tone 2 Frequency

Format: 16 bits, unsigned

Equation: N = 8.192 x Frequency (in Hz)

Convert N to hexadecimal then store in RAM.

12. Tone 1 Transmit Output Attenuation

13. Tone 2 Transmit Output Attenuation

Format: 16-bits, positive, twos complement

Calculate the output attenuation of each tone independently by using the equation for SCP LINEOUT and SPKP/SPKM Attenuation (No. 2).

14. FDSP Microphone AGC Reference Level

Energy reference level for microphone AGC in speakerphone operation. When microphone signal energy is below the AGC reference level, a gain will be added until the signal energy after AGC reaches the reference level. When microphone signal energy is greater than the AGC reference level, a loss will be inserted until the signal energy after AGC drops to the reference level.

Format: 16 bits, positive, twos complement

Equation: Level = $(10^{[x/20]})(32767)$

Where: x = desired level in dB.

Range: 040Ch - 16C3h (-30 dB to -15 dB)

Default: 16C3h (-15 dB)

15. FDSP Microphone AGC Slew Rate

The AGC slew rate determines how rapidly the AGC algorithm tracks the microphone input speech signal. Larger/smaller slew rate values correspond to faster/slower average energy convergence to the AGC reference level.

Format: 16 bits, positive, twos complement

Range: 0098h - 04C0h

Default: 0260h

16. FDSP Microphone Speech Hangover

To avoid clipping of microphone input speech, the microphone channel remains open for a programmable period of time after speech is no longer detected (hangover).

Format: 16 bits, positive, twos complement

Equation: Hangover = 8 * x

Where: x = desired hangover time in ms.

Range: 0001h - 0FA0h

Default: 0400h (128 ms)

17. FDSP Speaker Speech Hangover

To avoid clipping of speaker output speech, the speaker channel remains open for a programmable period of time after speech is no longer detected (hangover).

Format: 16 bits, positive, twos complement

Equation: Hangover = 8 * x

Where: x = desired hangover time in ms.

Range: 0001h - 0FA0h

Default: 04B0h (150 ms)

4.3 INTEGRATED ANALOG CONTROL REGISTERS

The RCSCP2 has an internal integrated analog front end (IA) which provides filtering, internal analog switching, and an internally sourced microphone bias output. The IA is controlled by three registers, located in internal RAM-space, which are accessed via the RCSCP2 interface memory. These registers provide individual controls for the IA's two inputs and two outputs, and control of all internal analog switching. The registers are located in internal RAM as shown in Table 4-2. The LSB of each 16-bit address's contents is used to control the IA.

Table 4-2. IA RAM Access Codes

Register	Name	CR	IO	ADD	IA Reg.	Default
IACR1	Input/Output Enable Register	0	0	94h	YDAL	BBh
IACR2	Speaker Output Control Register	0	0	98h	YDAL	08h
IACR3	Line Output Control Register	0	0	99h	YDAL	01h

Upon RCSCP2 reset or sleep wake-up, the three registers are initialized to default values (see Table 4-2). Each bit of each IA control register controls a specific IA circuit, as described below. The bits are accessed via RCSCP2 RAM Access.

4.3.1 IA Input/Output Enable Register (IACR1)

The bits in the IA Input/Output Enable Register (IACR1) control LINEOUT enable, SPKP/SPKM enable, LINEIN enable, and MICIN enable, as well as an optional 6 dB gain boost for the outputs, a 0-20 dB pre-amp gain for the MICIN, and a 4 dB attenuation for the LINEIN and MICIN inputs to the RCSCP2 (which is used when summing the inputs to prevent overloading the RCSCP2 input). Table 4-3 shows the bit signals.

Table 4-3. IA Input/Output Enable Register (IACR1) Bit Format

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IACR1	DAC Gain Enable 1 =6 dB Gain	MICIN Preamp Gain 00 = 0 dB Gain 01 = 10 dB Gain 10 = 15 dB Gain 11 = 20 dB Gain		LINEOUT Enable 1 = Enable	SPKP/SPKM Enable 1 = Enable	ADC Atten. 1 = 4 dB Atten.	LINEIN Enable 1 = Enable	MICIN Enable 1 = Enable

Bit 7 DAC Gain Enable

When control bit DAC Gain is enabled, the RCSCP2 output level is boosted by 6 dB in the DAC. When disabled, the output level boost is disabled (0 dB). By default, the IA DAC Gain is enabled.

Bits 6-5 Microphone (MICIN) Preamp Gain

Control bits 6 and 5, the MICIN Preamp Gain, select one of four amplifications for the MICIN pin, from 0 to 20 dB as shown. Default is 0 dB.

Bit 4 Line Output (LINEOUT) Enable

When control bit LINEOUT Enable is a 1, the line output driver in the IA is powered up and enabled. When LINEOUT Enable is a 0, and SPKP/SPKM Enable is a 0, the line output driver is powered down and tristated. By default, LINEOUT is enabled.

Bit 3 Speaker Output (SPKP/SPKM) Enable

When control bit SPKP/SPKM Enable is a 1, the speaker output drivers in the IA are powered up and enabled. When SPKP/SPKM Enable is a 0, the speaker output drivers are powered down and tristated. By default, SPKP/SPKM is disabled.

Bit 2 ADC Attenuation Enable

When control bit ADC Atten. is enabled, each input (MICIN and LINEIN) is attenuated by 4 dB prior to summation and analog to digital conversion, allowing larger signals at the two input pins without overloading the ADC. When ADC Atten. is disabled, no attenuation is performed on the input signals. Default is no attenuation.

Bit 1 Line Input (LINEIN) Enable

When control bit LINEIN Enable is a 1, the signal at the LINEIN pin is routed to the ADC input. When LINEIN Enable is a 0, the LINEIN signal is not connected to the ADC. By default, LINEIN is enabled.

Bit 0 Microphone Input (MICIN) Enable

When control bit MICIN Enable is a 1, the signal at the MICIN pin is routed to the ADC input. When MICIN Enable is a 0, the MICIN signal is not connected to the ADC. By default, the MICIN is disabled.

4.3.2 IA Speaker Output Control Register (IACR2)

The bits in the Speaker Output Control Register control signal routing from either the Microphone input (MICIN) or the Line input (LINEIN) to the Speaker output (SPKP/SPKM), and output squelching. In addition, a Microphone Bias voltage select bit is included.

Table 4-4. IA Speaker Output Control Register (IACR2) Bit Format

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IACR2	___	___	___	___	___	RX Loop Control 00 = Loop Disabled 01 = MICIN to SPKP/SPKM 10 = LINEIN to SPKP/SPKM 11 = Speaker Squelch		MICBIAS Select 0 = 2.2V

Bits 7-3 Reserved (Do Not Alter)

Bits 2-1 Analog Receive (RX) Loop Control

These two loop control bits control which input is looped to the SPKP/SPKM speaker outputs. By default, both bits are set to 0 disabling the analog RX loops. When Bits 2 and 1 are set to 0 and 1, respectively, the microphone input (MICIN) is looped back to the speaker outputs. When the bits are 1 and 0, the line input (LINEIN) is looped to the speaker outputs. When both bits are set to 1, the speaker outputs are clamped to AGND.

Bit 0 Microphone Bias (MICBIAS) Select

When control bit MICBIAS Select is a 1, the voltage present at the MICBIAS output is AGND. When MICBIAS is a 0, the provided microphone bias is 2.2V. By default, the IA is programmed to provide a 2.2V Microphone bias.

4.3.3 IA Line Output Control Register (IACR3)

The bits in the Line Output Control Register control signal routing from either the Microphone input, the Line input, or the RCSCP2 TX output to the Line output.

Table 4-5. IA Line Output Control Register (IACR3) Bit Format

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IACR3	___	___	___	___	___	___	TX Loop Control 00 = RCSCP2 to LINEOUT 01 = RCSCP2 to LINEOUT 10 = LINEIN to LINEOUT 11 = MICIN to LINEOUT	

Bits 7-2 Reserved (Do Not Alter)

Bits 1-0 Analog Transmit (TX) Loop Control

These two loop control bits control which input is looped to the LINEOUT line output. When bits 1 and 0 are both set to 0, or to 0 and 1, respectively, the RCSCP2 output is routed to the line output. When the bits are 1 and 0, the LINEIN line input is looped to the LINEOUT. When both bits are set to 1, the MICIN microphone input is looped to the LINEOUT. By default, the loop control is set to 01.

5. OPERATION

This section describes the operation of the RCSCP2 configurations and modes. Common codec operation is described first then specific codec configurations. Other configurations/modes/functions are then described.

5.1 CODEC CONFIGURATION SELECTION AND GENERAL PROCESSING

This section describes the operation of the speech codec configurations in terms of host use. A basic configuration and mode transition diagram is shown in Figure 5-1. Host processing flowcharts for recommended RCSCP2 general processing is illustrated in Figure 5-2.

The host selects the configuration by writing a configuration code to the CONF (06:0-7) control register then setting bit NEWC (1F:0). Setting of bit NEWC causes the RCSCP2 to exit the current configuration and enter the configuration corresponding to the CONF code. Control bits and RAM parameters are reset to default states when NEWC is set (see Table 3-2).

5.1.1 Handset/Headset/FDSP Mode and I/O Line Selection

The selected codec configuration operates in the Handset Mode with supporting LINEIN and LINEOUT lines, the Headset Mode with supporting MICIN and SPKP/SPKM lines, or the FDSP Mode with supporting MICIN and SPKP/SPKM lines. The Handset and Headset modes support handset or headset use that allows private conversation. The FDSP Mode supports microphone and speaker use which allows hands free operation. (See Section 5.6 for additional information.)

5.1.2 Codec Operation with Memory Interface Registers

5.1.2.1 Speech Coding From Memory Interface Registers

All codecs code the sampled analog speech signal from the microphone (MICIN) pin or line input (LINEIN) pin. All codecs can also code sampled analog speech signals supplied by the host through the memory interface registers with a few following changes to the Coder operation.

In the codec configuration subroutine, set control bit HIOE (0D:1) before enabling the Coder. Do not enable the Decoder. Enable the R00A interrupt along with the enabling of the R10A interrupt. In the interrupt service processing, in response to the R00A interrupt, write the MSB of the 16-bit speech sample to memory interface register 01, write the LSB to register 00, and return from the interrupt.

5.1.2.2 Speech Decoding To Memory Interface Registers

All codecs route the decoded analog speech signal to the speaker output (SPKP/SPKM) pins or line output (LINEOUT) pin. All codecs can also write each decoded speech sample to the memory interface registers with a few following changes to the Decoder operation.

In the codec configuration subroutine, set control bit HIOE (0D:1) before enabling the Decoder. Do not enable the Coder. In the Decoder data processing subroutine, enable R00A interrupt each time the Decoder status bit DCDRDY (0B:0) is set. In the interrupt service processing, in response to the R10A interrupt, read the MSB of the 16-bit decoded speech sample from interface memory register 11, read the LSB from register 10, and return from the interrupt.

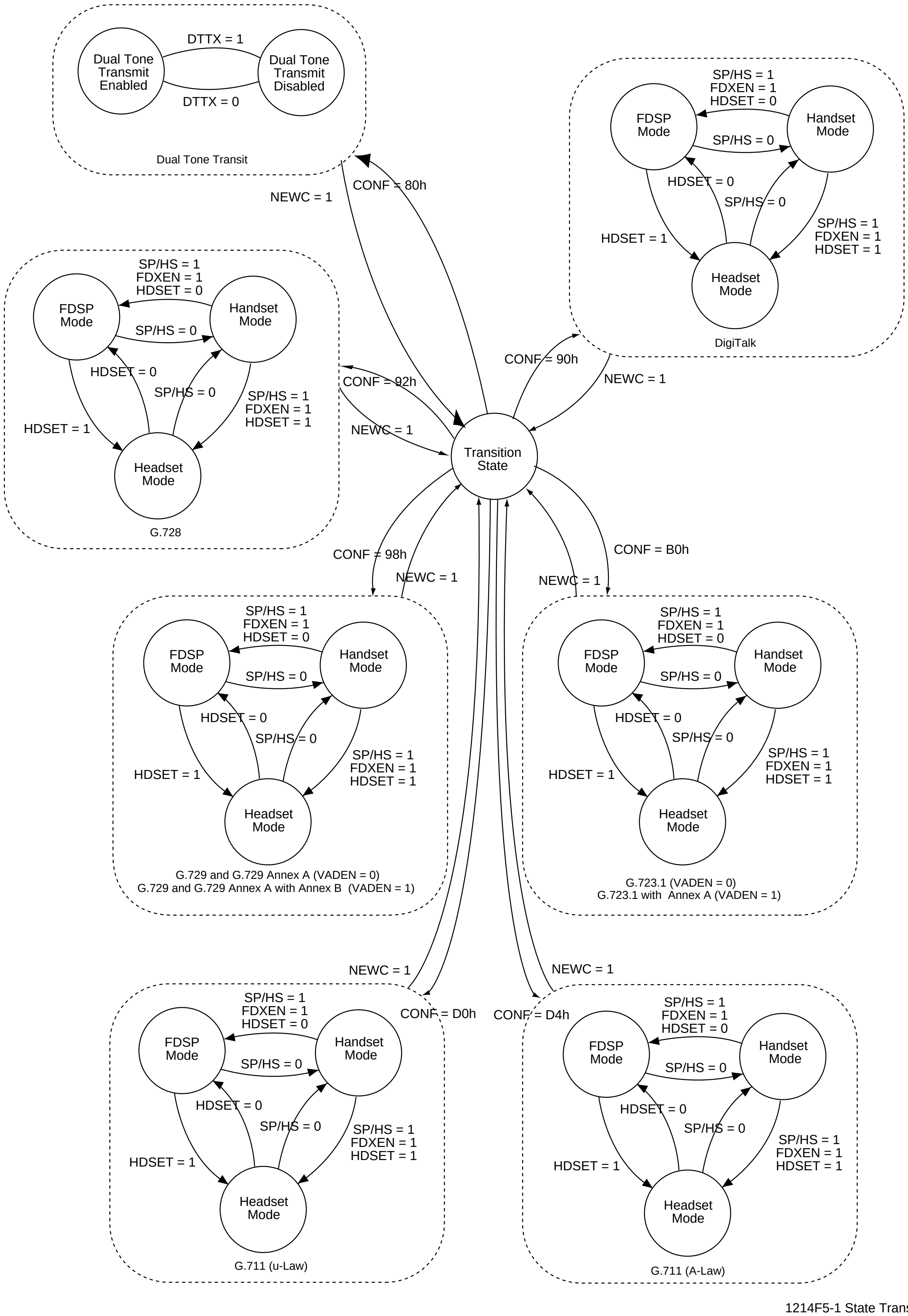

Figure 5-1. RCSCP2 Configuration and Mode Selection

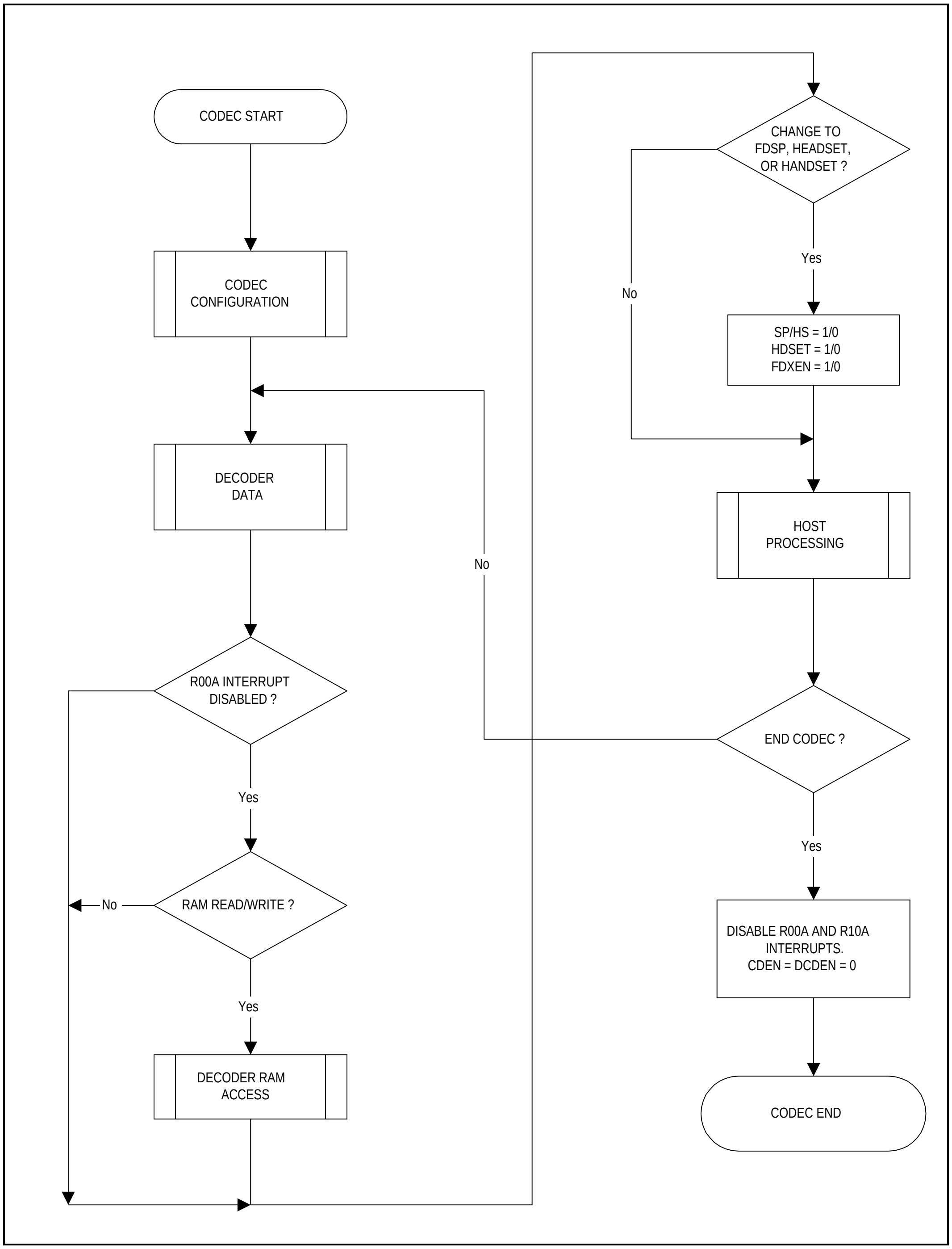

Figure 5-2. Host Flowchart - RCSCP2 Coder and Decoder General Processing

5.2 G.729 CODEC OPERATION

In G.729 Configuration, analog speech input on the LINEIN pin (Handset Mode) or MICIN pin (Headset or FDSP Mode) is converted to digital form, coded, and sent to a host when the Coder is enabled. Coded speech received from a host is decoded, converted to analog form, and output to the LINEOUT pin (Handset Mode) or SPKP/SPKM pins (Headset or FDSP Mode) pin when the Decoder is enabled. The Coder and Decoder can be enabled independently and simultaneously.

Host processing flowcharts for the G.729 Configuration are shown in Figure 5-3 (Codec Configuration Subroutine), Figure 5-4 (Decoder Data Subroutine), and Figure 5-5 (Interrupt Processing).

5.2.1 Configuration Entry and Exit

The host selects G.729 Configuration by writing 98h to control byte CONF (06) then setting bit NEWC (1F:0).

Resetting control bit VADEN (0C:0) selects G.729 and G.729 Annex A codec operation (see Section 5.2.4). Setting bit VADEN selects G.729 and G.729 Annex A with Annex B codec operation (see Section 5.2.5). VADEN can be set or reset anytime during codec operation.

5.2.2 Codec Control Bits

The following bits control codec operation:

CDEN	Enables/disables the Coder 1 = Enable, 0 = Disable.
DCDEN	Enables/disables the Decoder 1 = Enable, 0 = Disable.
APFEN	Enables/disables the Decoder Adaptive Postfilter. 1 = Enable, 0 = Disable.
FRMERA	Indicates frame erasure. 1 = Frame erased, 0 = Frame not erased.
VADEN	Enables/disables voice activity detector (VAD) 1 = Enable VAD, 0 = Disable VAD.
NTDCD	Specifies NT or VOICED/SID decoder input frame. 1 = NT frame, 0 = VOICED or SID frame.
SIDVDCD	Specifies VOICED or SID decoder input frame. 1 = VOICED frame, 0 = SID frame.

5.2.3 Codec Status Bits

The following bits report codec status:

NTENC	Indicates NT or VOICED/SID coder output frame 1 = NT frame, 0 = VOICED or SID frame.
SIDVENC	Indicates VOICED or SID coder output frame 1 = VOICED frame, 0 = SID frame.

5.2.4 G.729 and G.729 Annex A Codec Operation (VADEN = 0)

5.2.4.1 Coder

When the Coder is enabled, the analog speech signal on the LINEIN pin or MICIN pin is coded at 8.0 kbps and is presented to the host. The host enables the Coder by setting the Coder Enable control bit, CDEN (0C:4).

Coder Data Buffers (CDB1-CDB4). The coded speech data is presented to the host in a 4-4-2 sequence of two groups of four bytes followed by one group of two bytes (10 bytes total) every 10 ms. The coded speech data is loaded into the Coder Data Buffers; two groups of four bytes into CDB1 (13:0-7), CDB2 (12:0-7), CDB3 (11:0-7), and CDB4 (10:0-7), successively, followed by one group of two bytes into CDB3 and CDB4. Interrupt bit R10A (1E:3) is set and ~IRQ is asserted when CDB4 is loaded. The Coder writes the 4-4-2 sequence to CDB1-CDB4 in programmable multiples of 125 µs. The default value is 125 µs.

In response to each ~IRQ assertion, the host reads the coded speech data from CDB1, CDB2, CDB3, and CDB4 (four byte-group) or from CDB3 and CDB4 (two-byte group), successively. Reading CDB4 resets R10A. The host must read all 10 bytes of coded speech data within 10 ms, otherwise the codec will pause until the data transfer is complete.

5.2.4.2 Decoder

When the Decoder is enabled, coded speech received from the host is decoded and routed to the LINEOUT pin or SPKP/SPKM pins. The host enables the Decoder by setting the Decoder Enable control bit, DCDEN (0C:5). The host must set bit SIDVDCD (0D:3) and reset bit NTDCD (0D:2) before enabling the Decoder.

Decoder Data Buffers (DCDB1-DCDB4). After receiving the error-free 10-byte coded speech frame, the host enables assertion of ~IRQ.

The RCSCP2 sets status bit R00A (1E:0) (and asserts ~IRQ) to indicate empty Decoder Data Buffers, DCDB1 (03:0-7), DCDB2 (02:0-7), DCDB3 (01:0-7), and DCDB4 (00:0-7). Responding to the first of three R00A ~IRQ assertions, the host resets the Frame Erasure status bit, FRMERA (0C:6). The host writes two groups of four bytes to DCDB1, DCDB2, DCDB3, and DCDB4, successively, in response to the first two interrupts, and one group of two bytes to DCDB3 and DCDB4 in response to the third interrupt. Writing to DCDB4 resets bit R00A. On the third and final interrupt, the host disables the R00A ~IRQ interrupt before writing the 10th and last byte of the coded speech frame to DCDB4.

Frame Erasure. If the host detects bit error(s) in the received coded speech frame, the host enables the ~IRQ interrupt, then in response to the ~IRQ interrupt, sets bit FRMERA (0C:6) to indicate frame erasure, disables the ~IRQ interrupt, and reads from or writes to DCDB4 (00:0-7) to reset bit R00A (1F:0). There is no coded speech data transfer.

Decoder Timing Recovery. The Decoder robust timing recovery algorithm compensates for sample clock skew between the remote coder and local Decoder, asynchronous host-to-decoder coded speech data transfer delay, intervening variable length data block transmission delay, and loss of coded speech data.

The host must send each coded speech frame as soon as it is received from the coder. At no time should the host combine two or more coded frames before initiating data transmission.

Decoder Adaptive Postfilter. The Decoder adaptive postfilter may be enabled or disabled by the host setting or resetting the Adaptive Postfilter Enable control bit, APFEN (0C:7). The host may want to disable the adaptive postfilter for tandem codings.

5.2.5 G.729 and G.729 Annex A with G.729 Annex B Codec Operation (VADEN = 1)

5.2.5.1 Coder

When the Coder is enabled, the analog speech signal on the LINEIN pin or MICIN pin is coded at an average bit rate significantly lower than 8.0 kbps and is presented to the host. The host enables the Coder by setting the Coder Enable control bit, CDEN (0C:4).

1. Coder Data Buffers (CDB1-CDB4)

VOICED Frame. The Coder sets bit SIDVENC (0A:1) and resets bit NTENC (0A:0).

The coded speech data is presented to the host in a 4-4-2 sequence of two groups of four bytes followed by one group of two bytes (10 bytes total) every 10 ms. The coded speech data is loaded into the Coder Data Buffers; two groups of four bytes into CDB1 (13:0-7), CDB2 (12:0-7), CDB3 (11:0-7), and CDB4 (10:0-7), successively, followed by one group of two bytes into CDB3 and CDB4. Interrupt bit R10A (1E:3) is set and ~IRQ is asserted when CDB4 is loaded. The Coder writes the 4-4-2 sequence to CDB1-CDB4 in programmable multiples of 125 µs. The default value is 125 µs.

In response to each ~IRQ assertion, the host reads the coded speech data from CDB1, CDB2, CDB3, and CDB4 (four byte-group) or from CDB3 and CDB4 (two-byte group), successively. Reading CDB4 resets R10A. The host must read all 10 bytes of coded speech data within 10 ms, otherwise the codec will pause until the data transfer is complete.

SID Frame. The Coder resets bits SIDVENC (0A:1) and NTENC (0A:0).

The coded speech data is presented to the host in one group of two bytes every 10 ms. The coded speech data is loaded into the Coder Data Buffers CDB3 (11:0-7) and CDB4 (10:0-7). Interrupt bit R10A (1E:3) is set and ~IRQ is asserted when CDB4 is loaded. The Coder writes the 2-byte group to CDB3 and CDB4 in programmable multiples of 125 µs. The default value is 125 µs.

In response to each ~IRQ assertion, the host reads the coded speech data from CDB3 and CDB4. Reading CDB4 resets R10A. The host must read both bytes of coded speech data within 10 ms, otherwise the codec will pause until the data transfer is complete.

NT Frame. The Coder resets bit SIDVENC (0A:1) and sets bit NTENC (0A:0).

In response to the ~IRQ assertion, the host reads from, or writes to, CDB4 (10:0-7) to reset R10A (1E:3). There is no data to be transferred to the host.

5.2.5.2 Decoder

When the Decoder is enabled, coded speech received from the host is decoded and routed to the LINEOUT pin or SPKP/SKPN pins. The host enables the Decoder by setting the Decoder Enable control bit, DCDEN (0C:5).

1. Decoder Data Buffers (DCDB1-DCDB4)

VOICED Frame. After receiving the error-free 10-byte coded VOICED speech frame, the host sets bit SIDVDCD (0D:3), resets bit NTDCD (0D:2), and enables assertion of ~IRQ.

The RCSCP2 sets status bit R00A (1E:0) (and asserts ~IRQ) to indicate empty Decoder Data Buffers, DCDB1 (03:0-7), DCDB2 (02:0-7), DCDB3 (01:0-7), and DCDB4 (00:0-7). Responding to the first of three R00A ~IRQ assertions, the host resets the Frame Erasure status bit, FRMERA (0C:6). The host writes two groups of four bytes to DCDB1, DCDB2, DCDB3, and DCDB4, successively, in response to the first two interrupts, and one group of two bytes to DCDB3 and DCDB4 in response to the third interrupt. Writing to DCDB4 resets bit R00A. On the third interrupt, the host disables the R00A ~IRQ interrupt before writing the 10th and last byte of the coded speech frame to DCDB4.

SID Frame. After receiving the error-free 2-byte coded SID speech frame, the host resets bit SIDVDCD (0D:3), resets bit NTDCD (0D:2), and enables assertion of ~IRQ.

The RCSCP2 sets status bit R00A (1E:0) (and asserts ~IRQ) to indicate empty Decoder Data Buffers, DCDB3 (01:0-7) and DCDB4 (00:0-7). Responding to the R00A ~IRQ assertion, the host resets Frame Erasure status bit FRMERA (0C:6). The host writes two bytes to Decoder Data Buffers DCDB3 and DCDB4. Writing to DCDB4 resets bit R00A. The host then disables the R00A ~IRQ interrupt before writing the second and last byte of the coded speech frame to DCDB4.

NT Frame. After receiving the NT frame, the host enables assertion of ~IRQ, then in response to the ~IRQ interrupt, resets bit SIDVDCD (0D:3), sets bit NTDCD (0D:2), disables the ~IRQ interrupt, and reads from or writes to DCDB4 (00:0-7) to reset bit R00A (1E:0). There is no coded speech data to be transferred to the Decoder.

2. Frame Erasure

If the host detects bit error(s) in the received coded speech frame, the host enables the ~IRQ interrupt, then in response to the ~IRQ interrupt, sets bit FRMERA (0C:6) to indicate frame erasure, disables the ~IRQ interrupt, and reads from or writes to DCDB4 (00:0-7) to reset bit R00A (1E:0). There is no coded speech data transfer.

3. Decoder Timing Recovery

The Decoder robust timing recovery algorithm compensates for sample clock skew between the remote coder and local Decoder, asynchronous host-to-decoder coded speech data transfer delay, intervening variable length data block transmission delay, and loss of coded speech data.

The host must send each coded speech frame as soon as it is received from the coder. At no time should the host combine two or more coded frames before initiating data transmission.

4. Decoder Adaptive Postfilter

The Decoder adaptive postfilter may be enabled or disabled by the host setting or resetting the Adaptive Postfilter Enable control bit, APFEN (0C:7). The host may want to disable the adaptive postfilter for tandem codings.

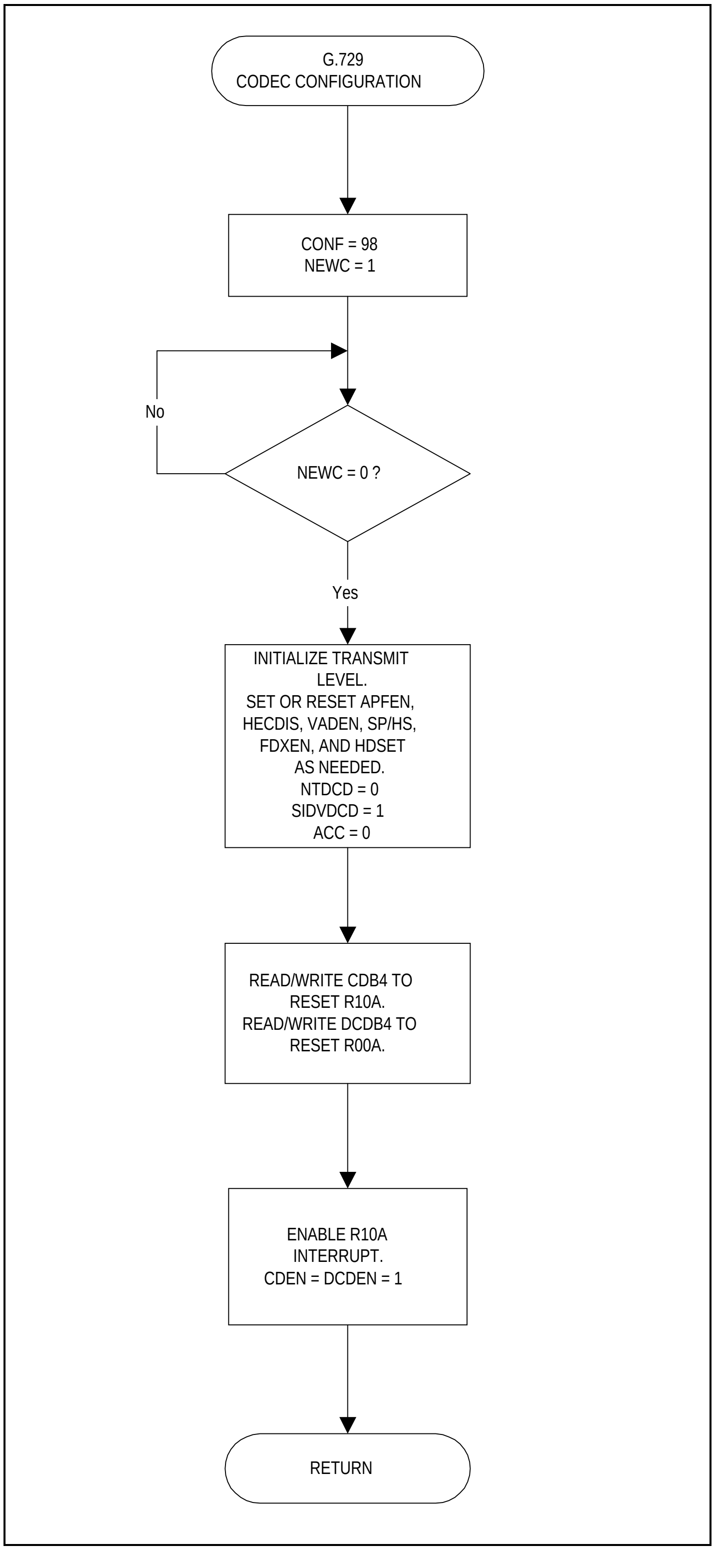

Figure 5-3. G.729 Codec Configuration Subroutine

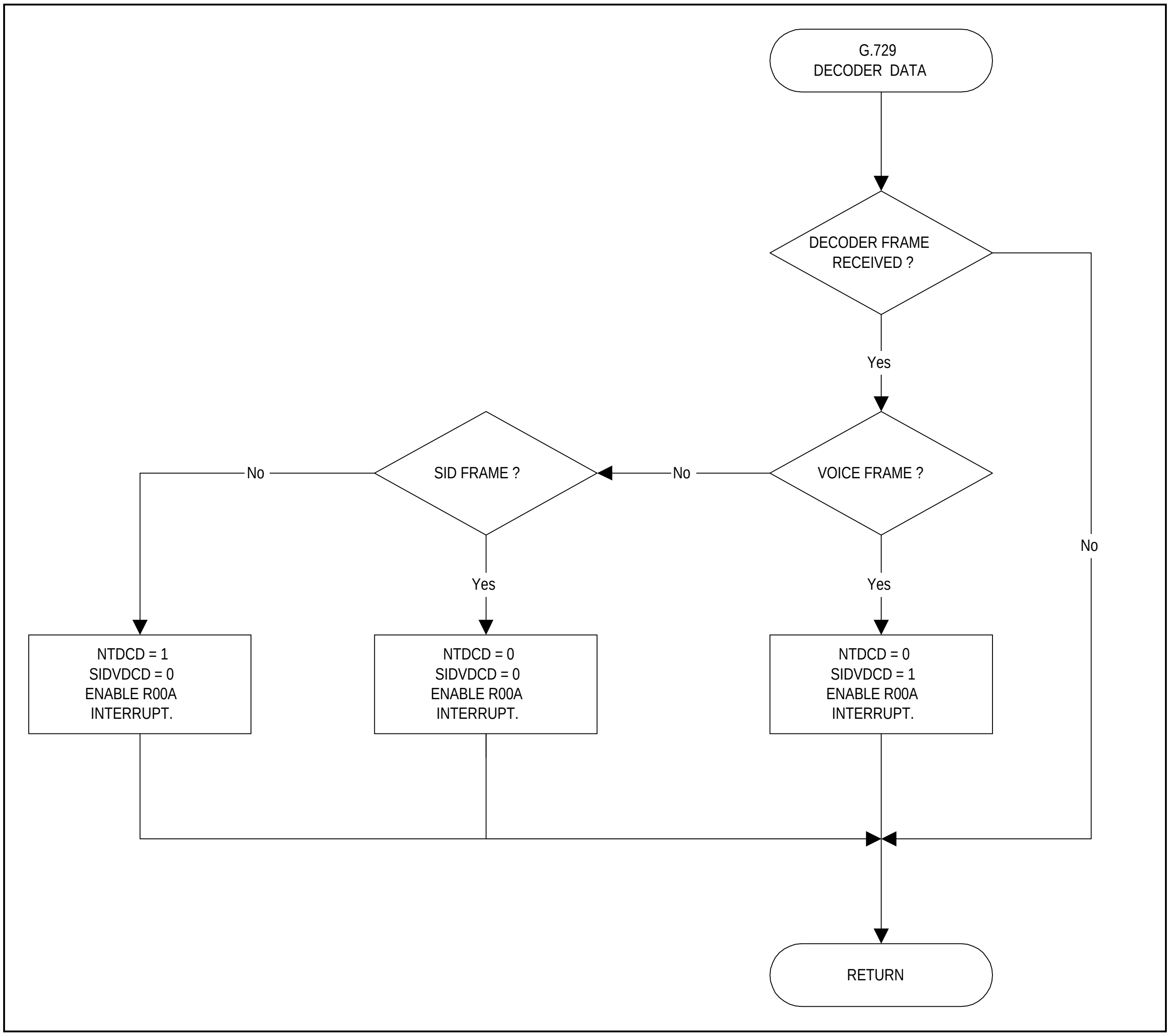

Figure 5-4. G.729 Decoder Data Subroutine

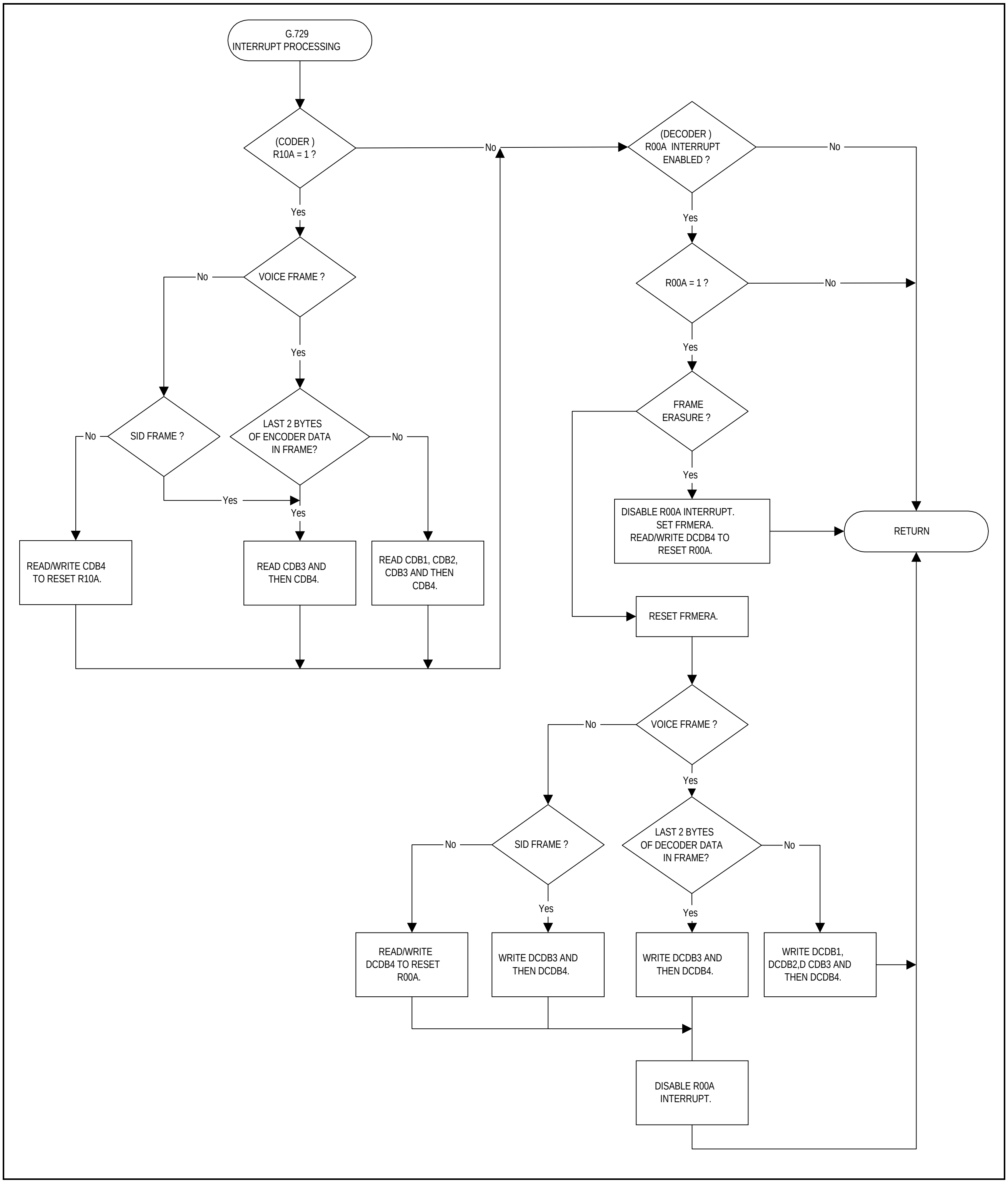

Figure 5-5. G.729 Interrupt Processing

5.3 G.723.1 CODEC OPERATION

In G.723.1 Configuration, analog speech input on the LINEIN pin (Handset Mode) or MICIN pin (Headset or FDSP Mode) is converted to digital form, coded, and sent to a host when the Coder is enabled; coded speech received from a host is decoded, converted to analog form, and output to the LINEOUT pin (Handset Mode) or SPKP/SPKM pins (Headset or FDSP Mode) pin when the Decoder is enabled. The Coder and Decoder can be enabled independently and simultaneously.

Host processing flowcharts for the G.723.1 Configuration are shown in Figure 5-6 (Codec Configuration Subroutine), Figure 5-7 (Decoder Data Subroutine), and Figure 5-8 (Interrupt Processing).

5.3.1 Configuration Entry and Exit

The host selects G.723.1 Configuration by writing B0h to control byte CONF (06) then setting bit NEWC (1F:0).

Resetting control bit VADEN (0C:0) selects G.723.1 codec operation (see Section 0). Setting bit VADEN selects G.723.1 with Annex A codec operation (see Section 5.3.5). VADEN can be set or reset anytime during codec operation.

5.3.2 Codec Control Bits

The following bits control mode operation:

CDEN	Enables/disables the Coder 1 = Enable, 0 = Disable.
DCDEN	Enables/disables the Decoder 1 = Enable, 0 = Disable.
APFEN	Enables/disables the Decoder Adaptive Postfilter. 1 = Enable, 0 = Disable.
FRMERA	Indicates frame erasure. 1 = Frame erased, 0 = Frame not erased.
VADEN	Enables/disables voice activity detector (VAD) 1 = Enable VAD, 0 = Disable VAD.
NTDCD	Specifies NT or VOICED/SID decoder input frame. 1 = NT frame, 0 = VOICED or SID frame.
DCRMEN	Enables/disables DC remover. 1 = Enable DC remover, 0 = Disable DC remover.
ENCR64	Selects Coder high or low rate. 1 = High rate, 0 = Low rate.

5.3.3 Codec Status Bits

The following status bits are updated during operation:

NTENC	Indicates NT or VOICED/SID coder output frame 1 = NT frame, 0 = VOICED or SID frame.

5.3.4 G.723.1 Codec Operation (VADEN = 0)

5.3.4.1 Coder

When the Coder is enabled, the analog speech signal on the LINEIN or MICIN pin is coded at 6.4 or 5.3 kbps and is presented to the host. The host enables the Coder by setting the Coder Enable control bit, CDEN (0C:4).

Coder Data Buffers (CDB1-CDB4). The host specifies the Coder bit rate using control bit ENCR64 (0C:3) (1 = high rate, 0 = low rate). The host may change the bit rate while the Coder is enabled. The number of bytes presented to the host every 30 ms depends upon the bit rate selection embedded in bit 0 of the first byte (0 = high rate, 1 = low rate). The coded speech data is presented to the host in six groups of four bytes (24 bytes total) for high rate or in five groups of four bytes (20 bytes total) for low rate.

The coded speech data is loaded into the Coder Data Buffers, CDB1 (13:0-7), CDB2 (12:0-7), CDB3 (11:0-7), and CDB4 (10:0-7), successively. Interrupt bit R10A (1E:3) is set and ~IRQ is asserted when CDB4 is loaded. The coder writes the six or five groups of four bytes to CDB1-CDB4 in programmable multiples of 125 µs. The default value is 125 µs.

In response to each ~IRQ assertion, the host reads the coded speech data from CDB1-CDB4, successively. Reading CDB4 resets R10A. The host must read all bytes of coded speech data within a 30 ms period, otherwise the codec will pause until data transfer is complete.

5.3.4.2 Decoder

When the Decoder is enabled, coded speech received from the host is decoded and routed to the LINEOUT pin or SPKP/SPKM pins. The host enables the Decoder by setting the Decoder Enable control bit, DCDEN (0C:5). The host must reset bit NTDCD (0D:2).

Decoder Data Buffers (DCDB1-DCDB4). After receiving the error-free coded 24-byte (high rate) or 20-byte (low rate) speech frame, the host enables the assertion of ~IRQ.

The RCSCP2 sets status bit R00A (1E:0) (and asserts ~IRQ) to indicate empty Decoder Data Buffers, DCDB1 (03:0-7), DCDB2 (02:0-7), DCDB3 (01:0-7), and DCDB4 (00:0-7). Responding to the first of six or five R00A ~IRQ assertions, the host resets the Frame Erasure status bit, FRMERA (0C:6). The host writes six or five groups of four bytes to DCDB1, DCDB2, DCDB3, and DCDB4, successively, in response to consecutive interrupts. The number of bytes within each frame depends upon the bit rate selection embedded in bit 0 of first byte of each coded frame (0 = high rate, 1 = low rate). The coded speech data is sent from the host in six groups of four bytes (24 bytes total) for high rate or in five groups of four bytes (20 bytes total) for low rate. On the final interrupt, the host disables the R00A ~IRQ interrupt before writing the last byte of coded speech frame to DCDB4.

5.3.5 G.723.1 with Annex A Codec Operation (VADEN = 1)

5.3.5.1 Coder

When the Coder is enabled, the analog speech signal on the LINEIN pin or MICIN pin is coded at an average bit rate significantly lower than 6.4/5.3 kbps and is presented to the host. The host enables the Coder by setting the Coder Enable control bit, CDEN (0C:4).

The number of bytes within each frame depends upon the bit rate selection indicated by bit 0 of the first byte in the frame, the SID/VOICED classification indicated by bit 1 of the first byte in the frame, and the NT status indicated by status bit NTENC (0A:0) (Table 5-6).

Table 5-6. G.723.1 Coder Bit Rate and Number of Bytes per Frame

NTENC Bit (0A:0)	Bit 0 of First Byte (Rate)	Bit 1 of First Byte (VAD)	Coder Rate	VAD Status	Number of Bytes per Frame
0	0	0	High rate	VOICED	24 bytes every 30 ms in 6 groups of 4 bytes
0	1	0	Low rate	VOICED	20 bytes every 30 ms in 5 groups of 4 bytes
0	0	1	N/A	SID	4 bytes every 30 ms in 1 group of 4 bytes
1	-	-	N/A	NT	0 bytes

1. Coder Data Buffers (CDB1-CDB4)

VOICED Frame. The number of bytes presented to the host every 30 ms depends upon the bit rate selection embedded in bit 0 of the first byte (0 = high rate, 1 = low rate). The coded speech data is presented to the host in six groups of four bytes (24 bytes total) for high rate or in five groups of four bytes (20 bytes total) for low rate.

The coded speech data is loaded into the Coder Data Buffers, CDB1 (13:0-7), CDB2 (12:0-7), CDB3 (11:0-7), and CDB4 (10:0-7), successively. Interrupt bit R10A (1E:3) is set and ~IRQ is asserted when CDB4 is loaded. The coder writes the six or five groups of four bytes to CDB1-CDB4 in programmable multiples of 125 µs. The default value is 125 µs.

In response to each ~IRQ assertion, the host reads the coded speech data from CDB1-CDB4, successively. Reading CDB4 resets R10A. The host must read all bytes of coded speech data within a 30 ms period, otherwise the codec will pause until data transfer is complete.

SID Frame. The coded speech data is presented to the host in one group of four bytes every 30 ms.

The coded speech data is loaded into the Coder Data Buffers, CDB1 (13:0-7), CDB2 (12:0-7), CDB3 (11:0-7), and CDB4 (10:0-7). Interrupt bit R10A (1E:3) is set and ~IRQ is asserted when CDB4 is loaded. The coder writes the group of four bytes to CDB1-CDB4 in programmable multiples of 125 µs. The default value is 125 µs.

In response to each ~IRQ assertion, the host reads the coded speech data from CDB1-CDB4. Reading CDB4 resets R10A. The host must read all four bytes of coded speech data within 30 ms, otherwise the codec will pause until data transfer is complete.

NT Frame. In response to the ~IRQ assertion, the host reads from, or writes to, CDB4 (10:0-7) to reset R10A (1E:3). There is no data to be transferred to the host.

5.3.5.2 Decoder

When the Decoder is enabled, coded speech received from the host is decoded and output to the LINEOUT pin or SPKP/SPKM pins. The host enables the Decoder by setting the Decoder Enable control bit, DCDEN(0C:5).

The number of bytes within each frame depends upon the bit rate selection indicated by bit 0 of the first byte in the frame, the SID/VOICED classification indicated by bit 1 of the first byte in the frame, and the NT status indicated by control bit NTDCD (0D:2) (Table 5-7).

Table 5-7. G.723.1 Decoder Bit Rate and Number of Bytes per Frame

NTDCD Bit (0D:2)	Bit 0 of First Byte (Rate)	Bit 1 of First Byte (VAD)	Decoder Rate	VAD Status	Number of Bytes per Frame
0	0	0	High rate	VOICED	24 bytes every 30 ms in 6 groups of 4 bytes
0	1	0	Low rate	VOICED	20 bytes every 30 ms in 5 groups of 4 bytes
0	0	1	N/A	SID	4 bytes every 30 ms in 1 group of 4 bytes
1	-	-	N/A	NT	0 bytes

1. Decoder Data Buffers (DCDB1-DCDB4)

VOICED Frame. After receiving the error-free 24-byte (high rate) or 20-byte (low rate) coded VOICED speech frame, the enables assertion of ~IRQ.

The RCSCP2 sets the status bit R00A (1E:0) (and asserts ~IRQ) to indicate empty Decoder Data Buffers, DCDB1 (03:0-7), DCDB2 (02:0-7), DCDB3 (01:0-7), and DCDB4 (00:0-7). Responding to the first of six or five R00A ~IRQ assertions, the host resets the Frame Erasure status bit, FRMERA (0C:6). The host writes six or five groups of four bytes to DCDB1, DCDB2, DCDB3, and DCDB4, successively, in response to consecutive interrupts. The number of bytes within each frame depends upon the bit rate selection embedded in bit 0 of first byte of each coded frame (0 = high rate, 1 = low rate). The coded speech data is sent from the host in six groups of four bytes (24 bytes total) for high rate or in five groups of four bytes (20 bytes total) for low rate. On the final interrupt, the host disables the R00A ~IRQ interrupt before writing the last byte of coded speech frame to DCDB4.

SID Frame. After receiving the error-free 4-byte coded SID speech frame, the host enables assertion of ~IRQ.

The RCSCP2 sets status bit R00A (1E:0) (and asserts ~IRQ) to indicate empty Decoder Data Buffers, DCDB1 (03:0-7), DCDB2 (02:0-7), DCDB3 (01:0-7), and DCDB4 (00:0-7). Responding to the R00A ~IRQ assertions, the host resets the Frame Erasure status bit, FRMERA (0C:6). The host writes one group of four bytes to DCDB1, DCDB2, DCDB3, and DCDB4 in response to the interrupt. The host disables the R00A ~IRQ interrupt before writing the last byte of coded speech frame to DCDB4.

NT Frame. After receiving the NT frame, the host enables assertion of ~IRQ, then in response to the ~IRQ interrupt, sets bit NTDCD (0D:2), disables the ~IRQ interrupt, and reads from or writes to DCDB4 (00:0-7) to reset bit R00A (1E:0). There is no coded speech data to be transferred to the Decoder.

2. Frame Erasure

If the host detects bit error(s) in the received coded speech frame, the host enables the ~IRQ interrupt, then in response to the ~IRQ interrupt, sets status bit FRMERA (0C:6) to indicate frame erasure, disables the ~IRQ interrupt, and reads from or writes to DCDB4 (00:0-7) to reset bit R00A (1E:0). There is no coded speech data transfer.

3. Decoder Timing Recovery

The Decoder robust timing recovery algorithm compensates for sample clock skew between the remote coder and local Decoder, asynchronous host-to-decoder coded speech data transfer delay, intervening variable length data block transmission delay, and loss of coded speech data.

The host must send each coded speech frame as soon as it is received from the coder. At no time should the host combine two or more coded frames before initiating data transmission.

4. Decoder Adaptive Postfilter

The Decoder adaptive postfilter may be enabled or disabled by the host setting or resetting the Adaptive Postfilter Enable control bit, APFEN (0C:7). The host may want to disable the adaptive postfilter for tandem codings.

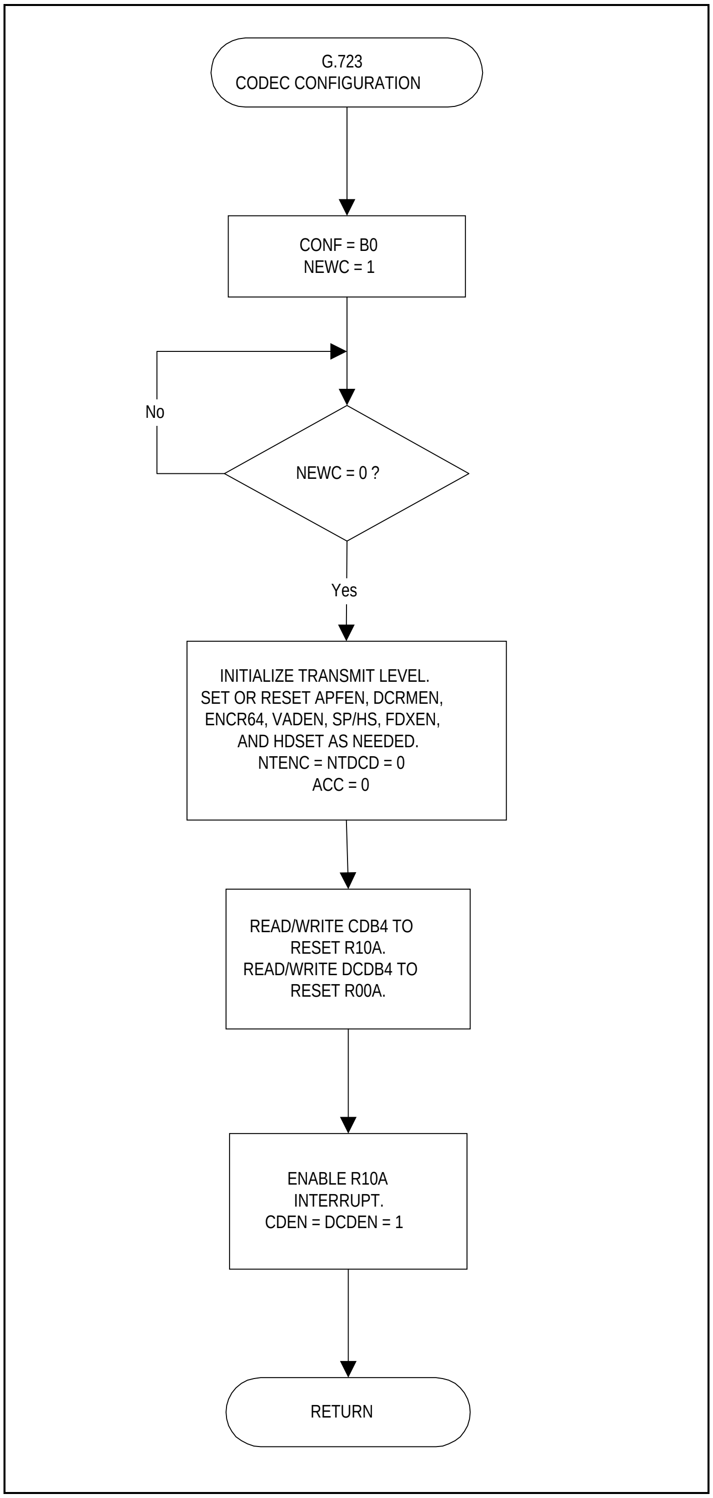

Figure 5-6. G.723.1 Codec Configuration

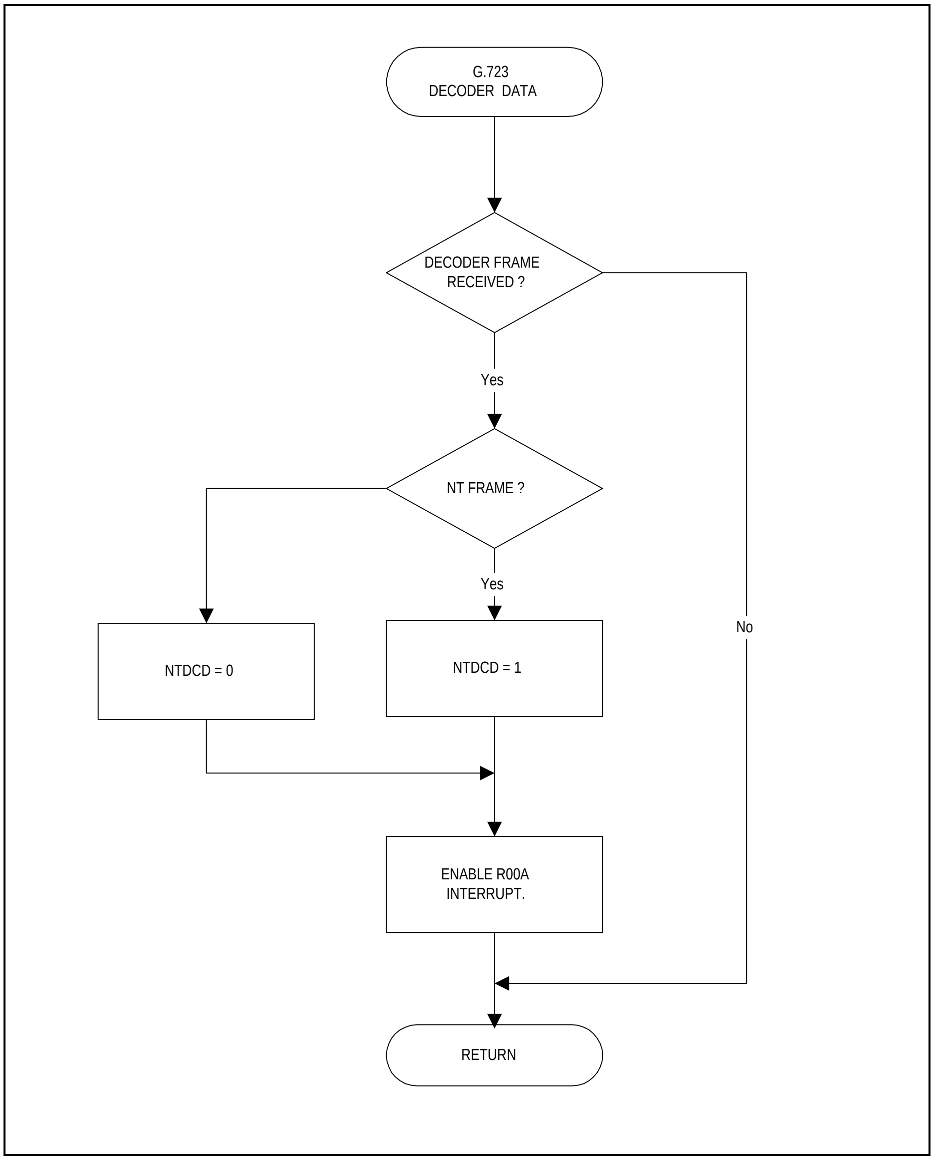

Figure 5-7. G.723.1 Decoder Data Subroutine

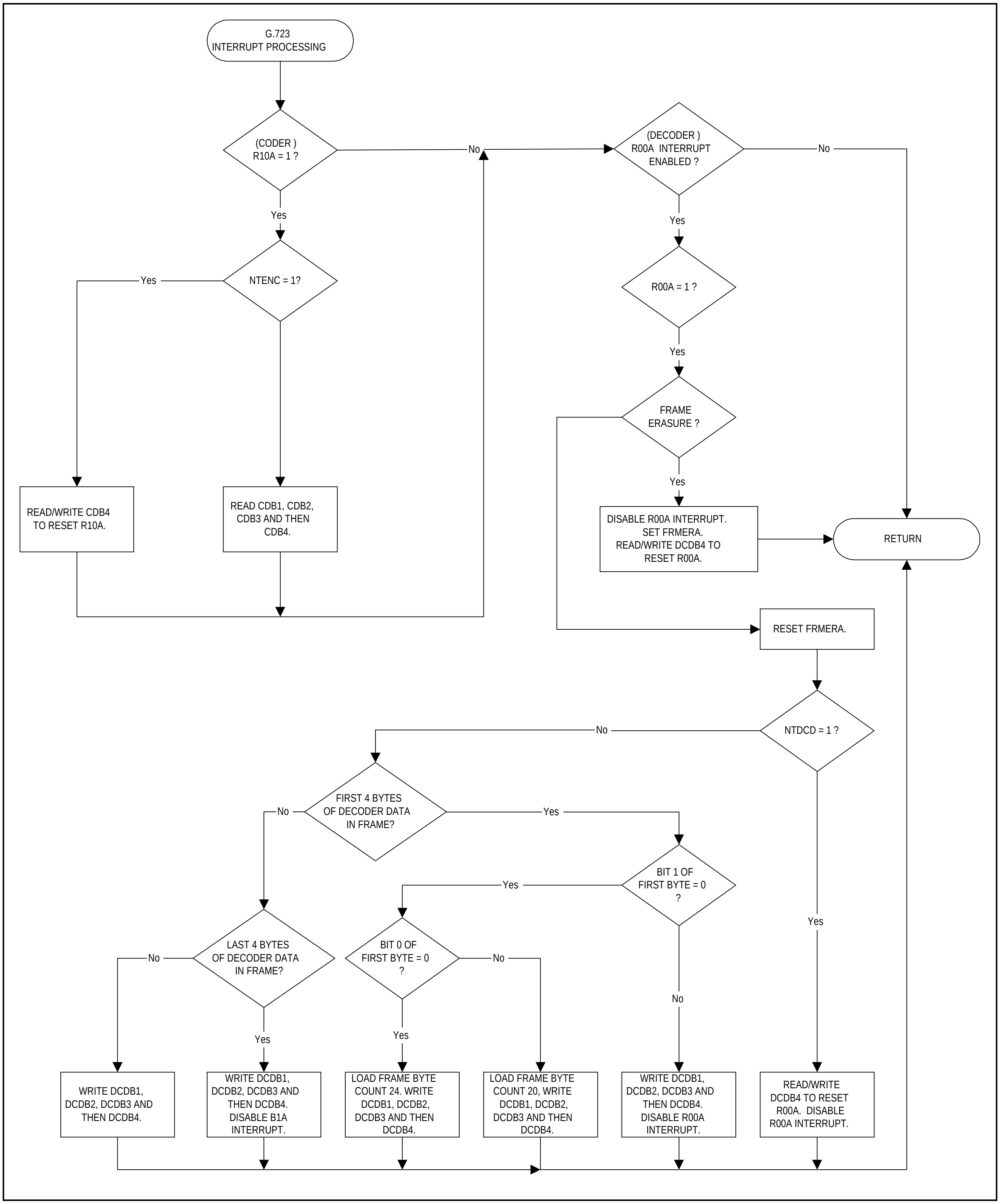

Figure 5-8. G.723.1 Interrupt Processing

5.4 DIGITALK CODEC OPERATION

In DigiTalk Configuration, analog speech input on the LINEIN pin (Handset Mode) or MICIN pin (Headset or FDSP Mode) is converted to digital form, coded, and sent to a host when the Coder is enabled; coded speech received from a host is decoded, converted to analog form, and output to the LINEOUT pin (Handset Mode) or SPKP/SPKM pins (Headset or FDSP Mode) pin when the Decoder is enabled. The Coder and Decoder can be enabled independently and simultaneously.

Host processing flowcharts for the DigiTalk Configuration are shown in Figure 5-9 (Codec Configuration Subroutine), Figure 5-10 (Decoder Data Subroutine), and Figure 5-8 (Interrupt Processing).

5.4.1 Configuration Entry and Exit

The host selects DigiTalk Configuration by writing 90h to control byte CONF (06:0-7) then setting bit NEWC bit (1F:0).

5.4.2 Codec Control Bits

The following bits control codec operation:

CDEN Enables/disables the RCSCP2 Coder
1 = Enable, 0 = Disable.

DCDEN Enables/disables the RCSCP2 Decoder
1 = Enable, 0 = Disable.

APFEN Enables/disables the RCSCP2 Decoder Adaptive Postfilter.
1 = Enable, 0 = Disable.

FRMERA Indicates frame erasure.
1 = Frame erased, 0 = Frame not erased.

VOXENC Controls delay of voice coding until VOX is set (to support voice activated coding).
1 = Delay coding until voice is detected, 0 = Do not delay voice coding.

5.4.3 Codec Status Bits

The following bits report codec status:

VOX Indicates presence or absence of speech when the coder is enabled.
1 = Voice present, 0 = voice absent.

5.4.4 DigiTalk Codec Operation

5.4.4.1 Coder

When the Coder is enabled, the analog speech signal on the LINEIN pin or MICIN pin is coded at 8.5 kbps and is presented to the host. The host enables the Coder by setting the Coder Enable Control bit, CDEN (0C:4).

Coder Data Buffers (CDB1-CDB4). The coded speech data is presented to the host in seven groups of four bytes (28 bytes total) every 26 ms. The coded speech data is loaded into the Coder Data Buffers, CDB1 (13:0-7), CDB2 (12:0-7), CDB3 (11:0-7), and CDB4 (10:0-7), successively. Interrupt bit R10A (1E:3) is set and ~IRQ is asserted when CDB4 is loaded. The coder writes four bytes of coded output speech data to the CDB1-CDB4 in programmable multiples of 125 µs. The default value is 125 µs.

In response to each ~IRQ assertion, the host reads the coded speech data from CDB1, CDB2, CDB3, and CDB4, successively. Reading CDB4 resets R10A. The host must read all 28 bytes of coded speech data within 26 ms, otherwise the Codec will pause until the data transfer is complete.

DigiTalk VOX Turn-On and Turn-Off Thresholds. The coder sets status bit VOX (0B:3) when the average energy of the speech signal being coded exceeds the VOX Turn-On Threshold. The coder resets bit VOX when the average energy is less than the VOX Turn-Off Threshold for a minimum period of time equal to the time constant of the energy averaging filter. The default value for this time constant is one-half second. The time constant may be changed by choosing new VOX energy averaging filter coefficients (see Section 4).

DigiTalk VOX Activated Encoding. If the VOX Activated Encoding control bit, VOXENC (0C:3), is set by the host before enabling the coder, the coder delays encoding of the speech signal until bit VOX is set.

Silence Deletion. Once bit VOX is reset and remains reset for a sufficient period of time (determined by the host), the host may choose to discard all coder output data until bit VOX is once again set. The host must still read all data from the coder, but does not need to transmit this data to the remote decoder. In the absence of coded speech data, the remote decoder inserts comfort noise. The comfort noise energy level is set equal to the previous frame's energy provided that this energy is less than or equal to a host programmable energy threshold. This threshold ranges from 0 to 31 with 0 representing silence and 31 representing the maximum possible energy output level (see Section 4).

5.4.4.2 Decoder

When the Decoder is enabled, coded speech received from the host is decoded and output to the LINEOUT pin or SPKP/SPKM pins. The host enables the Decoder by setting the Decoder Enable control bit, DCDEN (0C:5).

Decoder Data Buffers (DCDB1-DCDB4). After receiving the error-free 28-byte coded speech frame, the host enables assertion of ~IRQ.

The RCSCP2 sets status bit R00A status (1E:0) (and asserts ~IRQ) to indicate empty Decoder Data Buffers, DCDB1 (03:0-7), DCDB2 (02:0-7), DCDB3 (01:0-7), and DCDB4 (00:0-7). Responding to the first of seven R00A ~IRQ assertions, the host resets the Frame Erasure status bit, FRMERA (0C:6). The host writes four bytes to Decoder Data Buffers DCDB1, DCDB2, DCDB3, and DCDB4 on each consecutive interrupt. Writing to DCDB4 resets bit R00A. On the seventh and final interrupt, the host disables the R00A ~IRQ interrupt before writing the 28th and last byte of the coded speech frame to DCDB4.

Frame Erasure. If the host detects bit error(s) in the received coded speech frame, the host enables the ~IRQ interrupt, then in response to the ~IRQ interrupt, sets bit FRMERA (0C:6) to indicate frame erasure, disables the ~IRQ interrupt, and reads from or writes to DCDB4 (00:0-7) to reset bit R00A (1E:0). There is no coded speech data transfer.

Decoder Timing Recovery. The Decoder robust timing recovery algorithm compensates for sample clock skew between the remote coder and local Decoder, asynchronous host-to-Decoder coded speech data transfer delay, intervening variable length data block transmission delay, and loss of coded speech data.

The host must send each coded speech frame as soon as it is received from the coder. At no time should the host combine two or more coded frames before initiating data transmission.

Decoder Adaptive Postfilter. The Decoder adaptive postfilter may be enabled or disabled by the host setting or resetting the Adaptive Postfilter Enable control bit, APFEN (0C:7). The host may want to disable the adaptive postfilter for tandem codings.

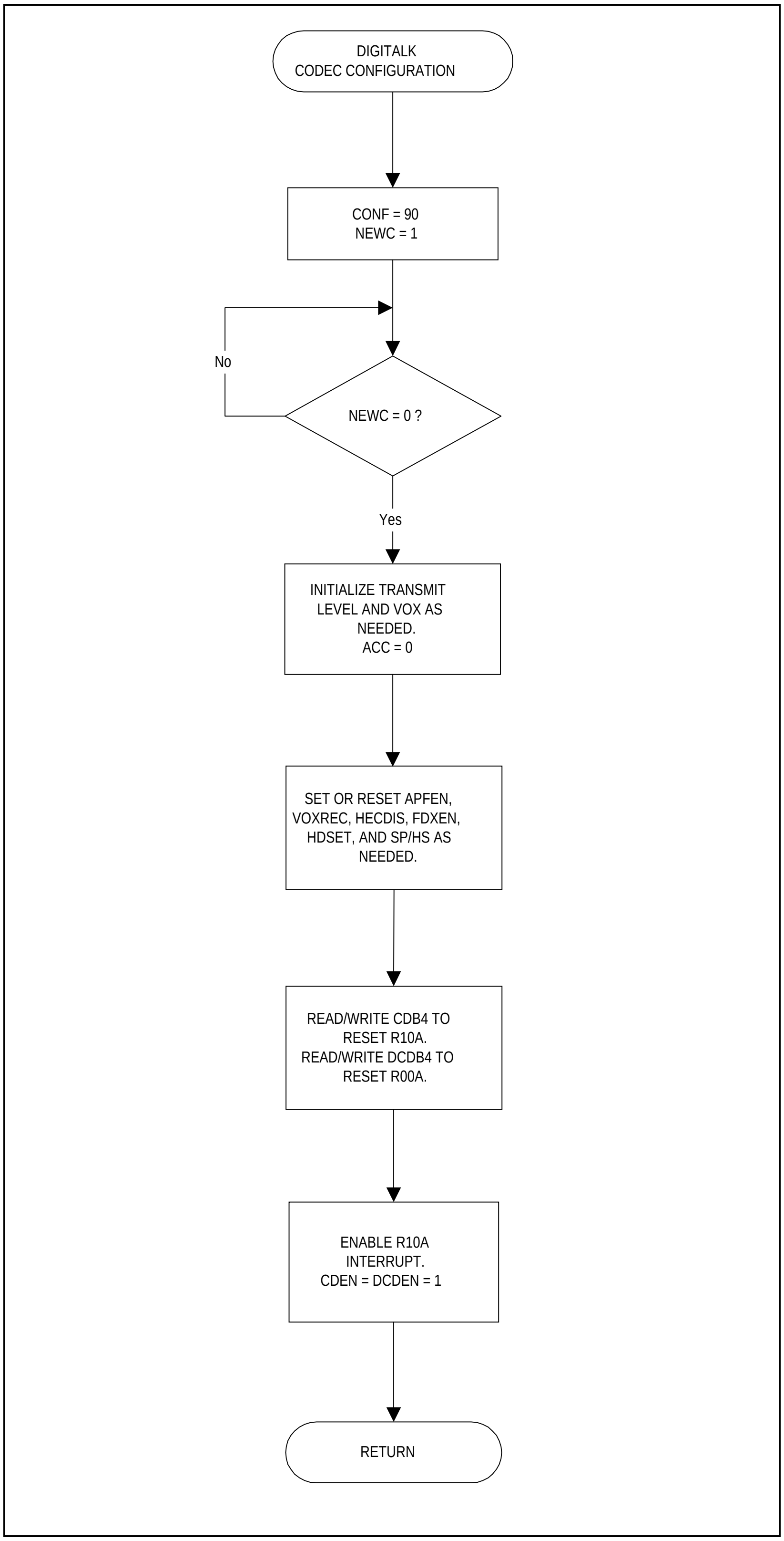

Figure 5-9. DigiTalk Codec Configuration Subroutine

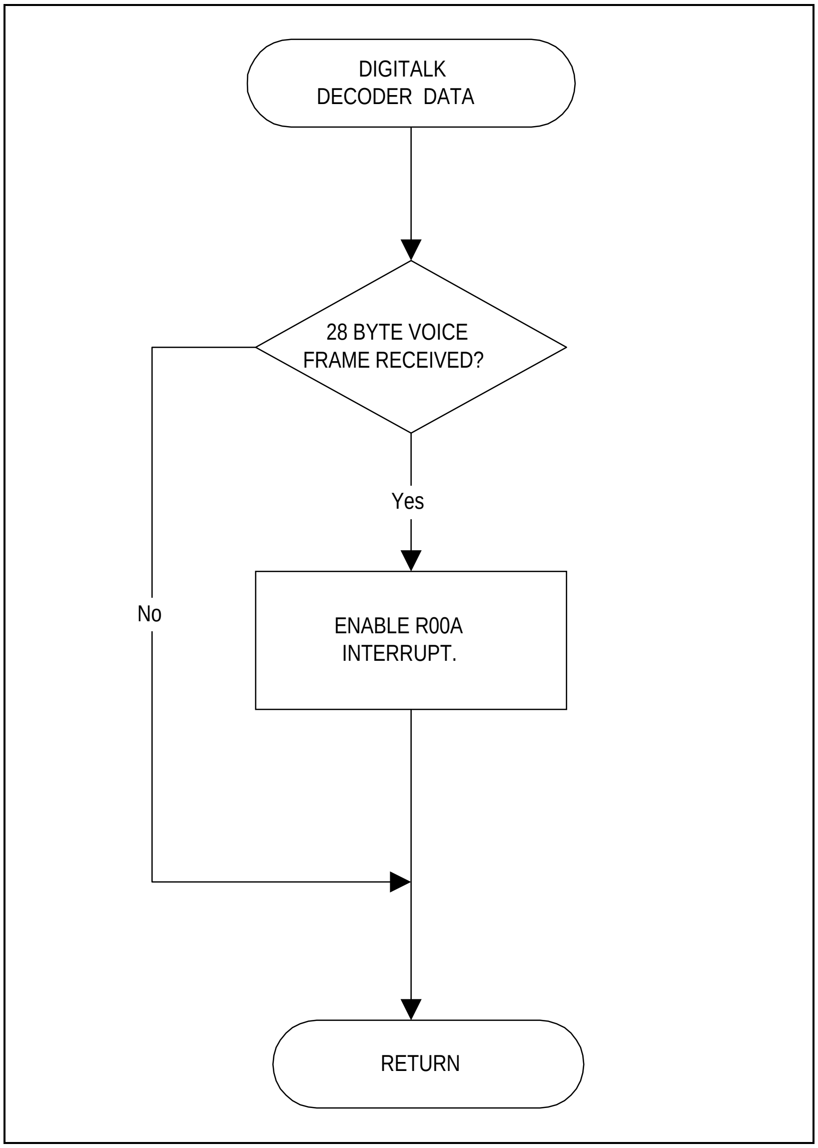

Figure 5-10. DigiTalk Decoder Data Subroutine

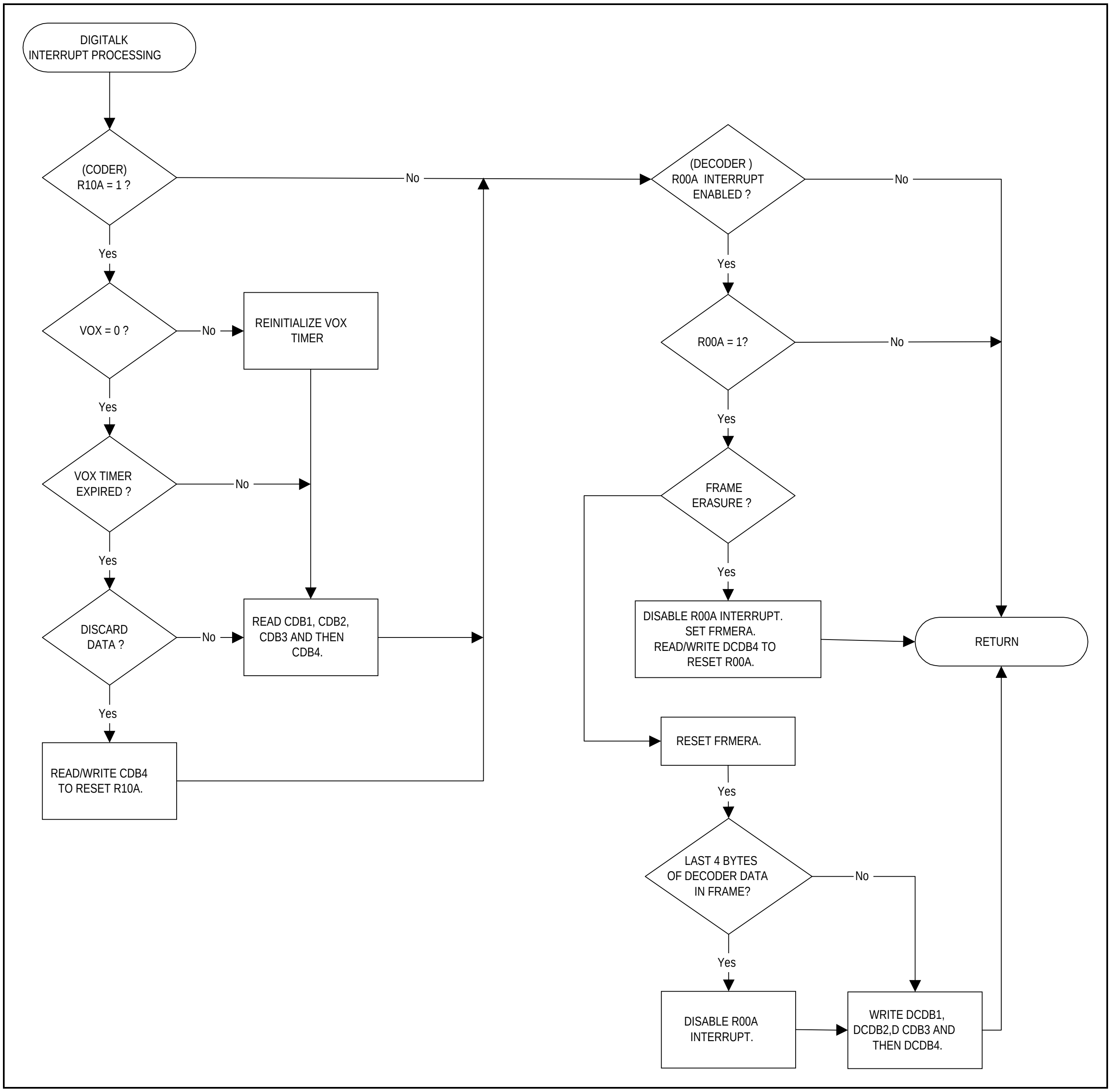

Figure 5-11. DigiTalk Interrupt Processing

5.5 G.711 CODEC OPERATION

In G.711 Configuration, analog speech input on the LINEIN pin (Handset Mode) or MICIN pin (Headset or FDSP Mode) is converted to digital form, coded, and sent to a host when the Coder is enabled; coded speech received from a host is decoded, converted to analog form, and output to the LINEOUT pin (Handset Mode) or SPKP/SPKM pins (Headset or FDSP Mode) pin when the Decoder is enabled. The Coder and Decoder can be enabled independently and simultaneously.

Host processing flowcharts for the G.711 Configuration are shown in Figure 5-12 (Codec Configuration Subroutine), Figure 5-13 (Decoder Data Subroutine), and Figure 5-14 (Interrupt Processing).

5.5.1 Configuration Entry and Exit

The host selects G.711 Configuration by writing D0h (μ-Law) or D4h (A-Law) to control byte CONF (06) then setting bit NEWC (1F:0).

5.5.2 Codec Control Bits

The following bits control mode operation:

CDEN Enables/disables the Coder
1 = Enable, 0 = Disable.

DCDEN Enables/disables the Decoder
1 = Enable, 0 = Disable.

5.5.3 Codec Status Bits

None.

5.5.4 G.711 Codec Operation (μ-Law and A-Law)

5.5.4.1 Coder

When the Coder is enabled, the analog speech signal on the LINEIN or MICIN pin is coded at 64 kbps and is presented to the host. The host enables the Coder by setting the Coder Enable control bit, CDEN (0C:4).

Coder Data Buffers (CDB1-CDB4). The coded speech data is presented to the host in 60 groups of four bytes (240 bytes total) every 30 ms. The coded speech data is loaded into the Coder Data Buffers; 60 groups of four bytes into CDB1 (13:0-7), CDB2 (12:0-7), CDB3 (11:0-7), and CDB4 (10:0-7), successively. Interrupt bit R10A (1E:3) is set and ~IRQ is asserted when CDB4 is loaded. The Coder writes the 60 groups of four bytes to CDB1-CDB4 in programmable multiples of 125 µs. The default value is 125 µs.

In response to each ~IRQ assertion, the host reads the coded speech data from CDB1, CDB2, CDB3, and CDB4 (four byte-group), successively. Reading CDB4 resets R10A. The host must read all 240 bytes of coded speech data within 30 ms, otherwise the codec will pause until the data transfer is complete.

5.5.4.2 Decoder

When the Decoder is enabled, coded speech received from the host is decoded and routed to the LINEOUT pin or SPKP/SPKM pins. The host enables the Decoder by setting the Decoder Enable control bit, DCDEN (0C:5).

Decoder Data Buffers (DCDB1-DCDB4). After receiving the error-free 240-byte coded speech frame, the host enables assertion of ~IRQ.

The RCSCP2 sets status bit R00A (1E:0) (and asserts ~IRQ) to indicate empty Decoder Data Buffers, DCDB1 (03:0-7), DCDB2 (02:0-7), DCDB3 (01:0-7), and DCDB4 (00:0-7). The host writes 60 groups of four bytes to DCDB1, DCDB2, DCDB3, and DCDB4, successively, in response to consecutive interrupts. Writing to DCDB4 resets bit R00A. On the 60th interrupt, the host disables the R00A ~IRQ interrupt before writing the 240th and last byte of the coded speech frame to DCDB4.

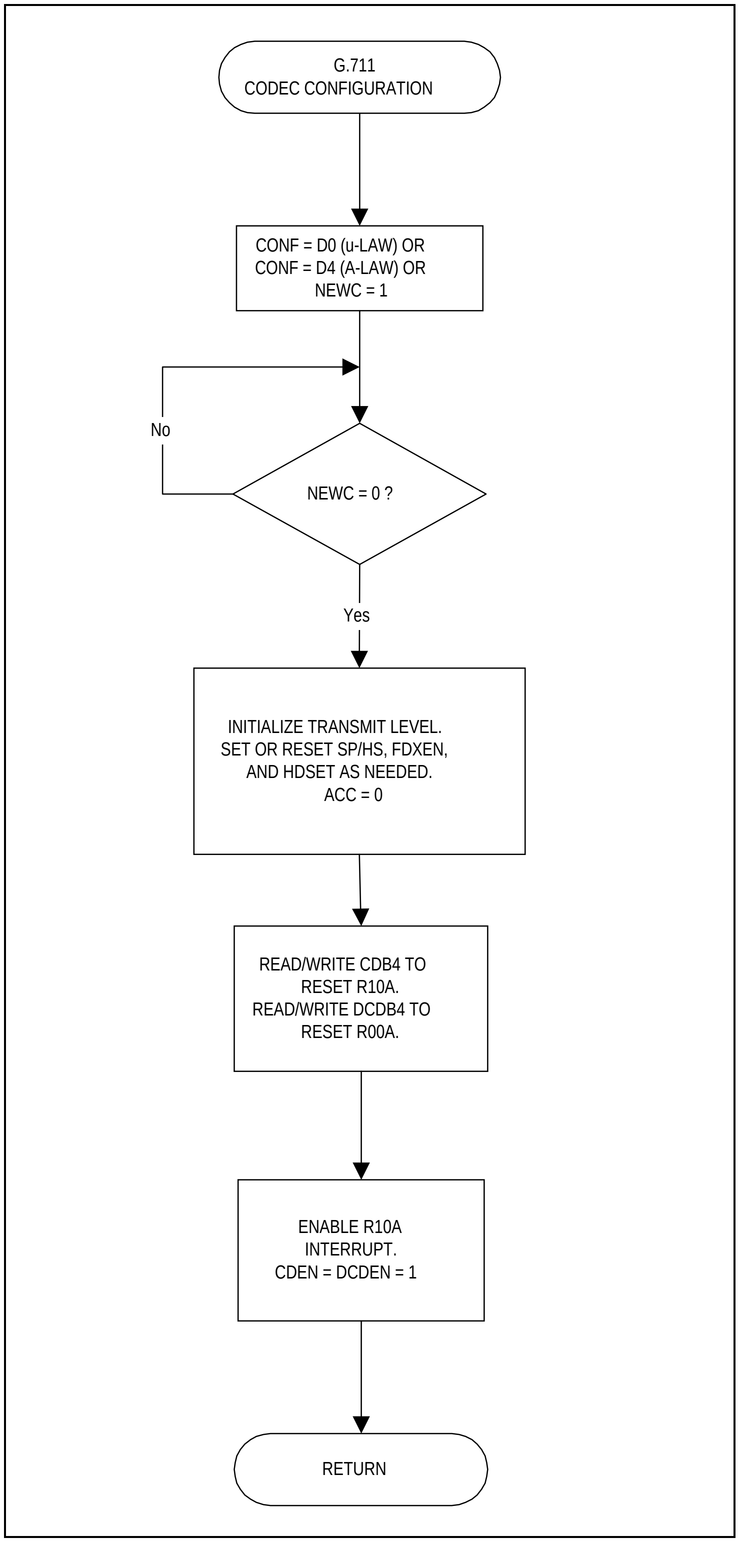

Figure 5-12. G.711 Codec Configuration

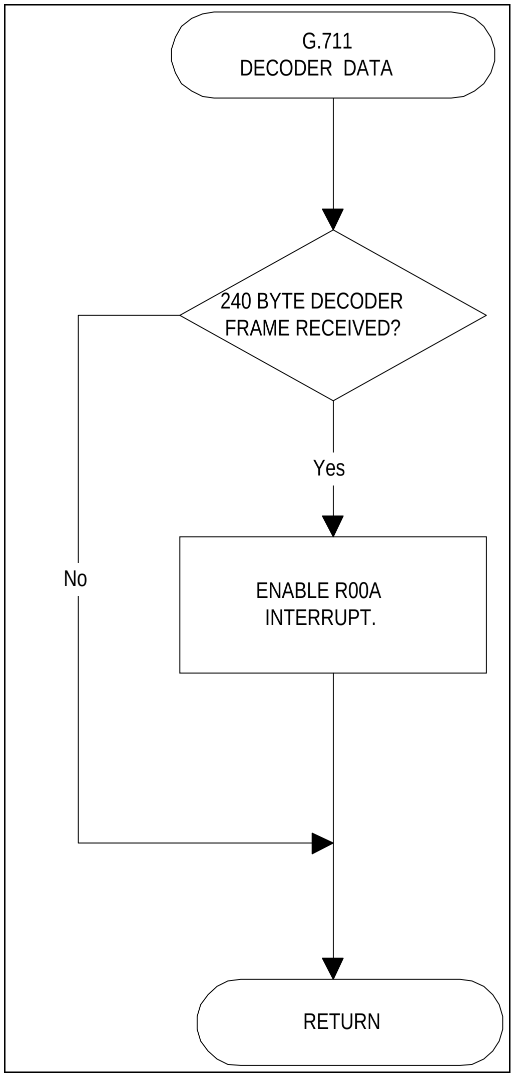

Figure 5-13. G.711 Decoder Data Subroutine

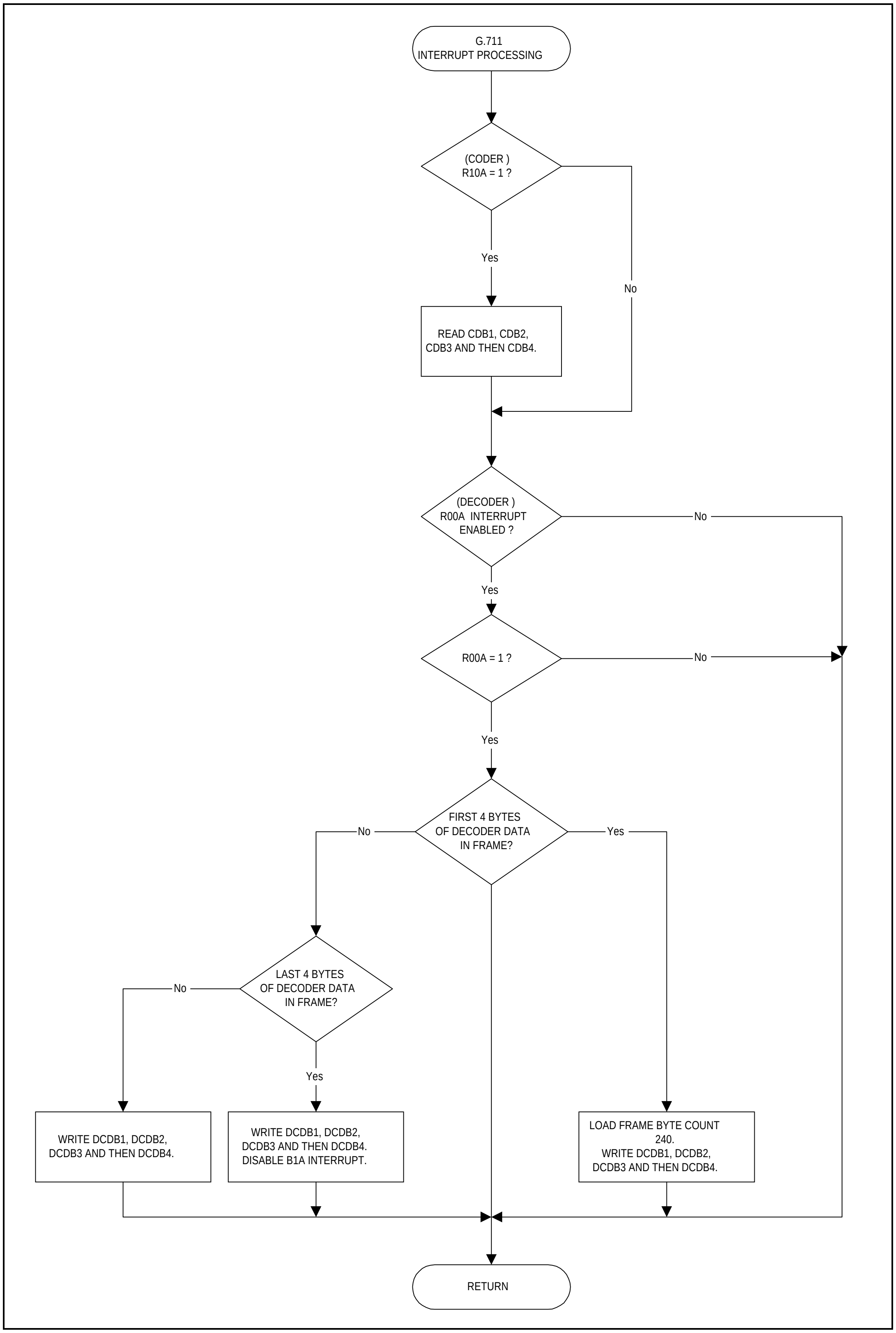

Figure 5-14. G.711 Interrupt Processing

5.6 G.728 CODEC OPERATION

In G.728 Configuration, analog speech input on the LINEIN pin (Handset Mode) or MICIN pin (Headset or FDSP Mode) is converted to digital form, coded, and sent to a host when the Coder is enabled; coded speech received from a host is decoded, converted to analog form, and output to the LINEOUT pin (Handset Mode) or SPKP/SPKM pins (Headset or FDSP Mode) pin when the Decoder is enabled. The Coder and Decoder can be enabled independently and simultaneously.

Host processing flowcharts for the G.728 Configuration are shown in Figure 5-15 (Codec Configuration Subroutine), Figure 5-16 (Decoder Data Subroutine), and Figure 5-17(Interrupt Processing).

5.6.1 Configuration Entry and Exit

The host selects G.728 Configuration by writing 92h to control byte CONF (06) then setting bit NEWC (1F:0).

5.6.2 Codec Control Bits

The following bits control mode operation:

CDEN Enables/disables the Coder
1 = Enable, 0 = Disable.

DCDEN Enables/disables the Decoder
1 = Enable, 0 = Disable.

5.6.3 Codec Status Bits

None.

5.6.4 G.728 Codec Operation

5.6.4.1 Coder

When the Coder is enabled, the analog speech signal on the LINEIN or MICIN pin is coded at 16 kbps and is presented to the host. The host enables the Coder by setting the Coder Enable control bit, CDEN (0C:4).

Coder Data Buffers (CDB1-CDB4). The coded speech data is presented to the host in 10 groups of four bytes (40 bytes total) every 20 ms. The coded speech data is loaded into the Coder Data Buffers; 10 groups of four bytes into CDB1 (13:0-7), CDB2 (12:0-7), CDB3 (11:0-7), and CDB4 (10:0-7), successively. Interrupt bit R10A (1E:3) is set and ~IRQ is asserted when CDB4 is loaded. The Coder writes the 10 groups of four bytes to CDB1-CDB4 in programmable multiples of 125 µs. The default value is 125 µs.

In response to each ~IRQ assertion, the host reads the coded speech data from CDB1, CDB2, CDB3, and CDB4 (four byte-group), successively. Reading CDB4 resets R10A. The host must read all 40 bytes of coded speech data within 20 ms, otherwise the codec will pause until the data transfer is complete.

5.6.4.2 Decoder

When the Decoder is enabled, coded speech received from the host is decoded and routed to the LINEOUT pin or SPKP/SPKM pins. The host enables the Decoder by setting the Decoder Enable control bit, DCDEN (0C:5).

Decoder Data Buffers (DCDB1-DCDB4). After receiving the error-free 40-byte coded speech frame, the host enables assertion of ~IRQ.

The RCSCP2 sets status bit R00A (1E:0) (and asserts ~IRQ) to indicate empty Decoder Data Buffers, DCDB1 (03:0-7), DCDB2 (02:0-7), DCDB3 (01:0-7), and DCDB4 (00:0-7). The host writes 10 groups of four bytes to DCDB1, DCDB2, DCDB3, and DCDB4, successively, in response to consecutive interrupts. Writing to DCDB4 resets bit R00A. On the 10th interrupt, the host disables the R00A ~IRQ interrupt before writing the 40th and last byte of the coded speech frame to DCDB4.

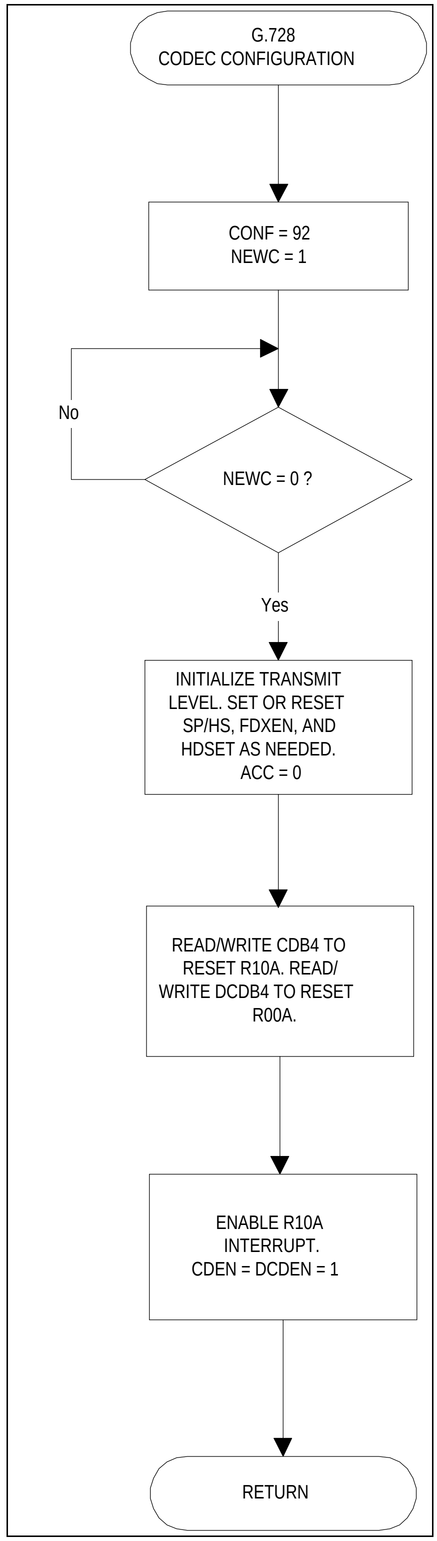

Figure 5-15. G.728 Codec Configuration

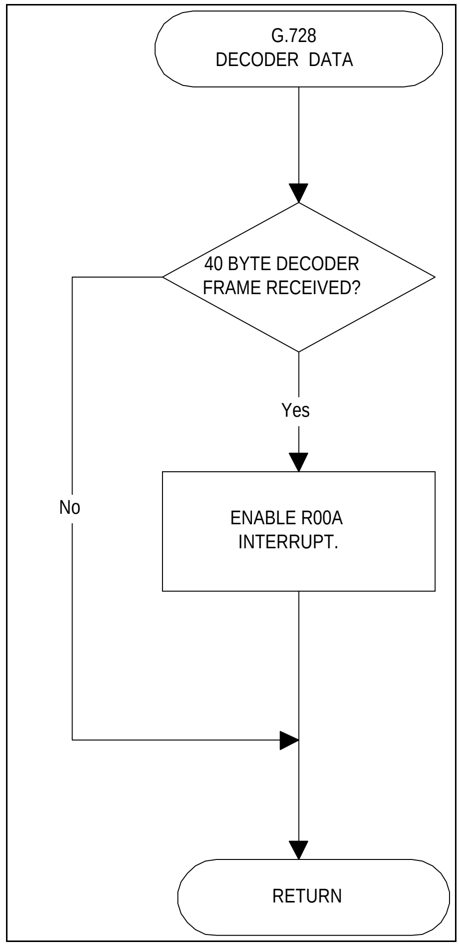

Figure 5-16. G.728 Decoder Data Subroutine

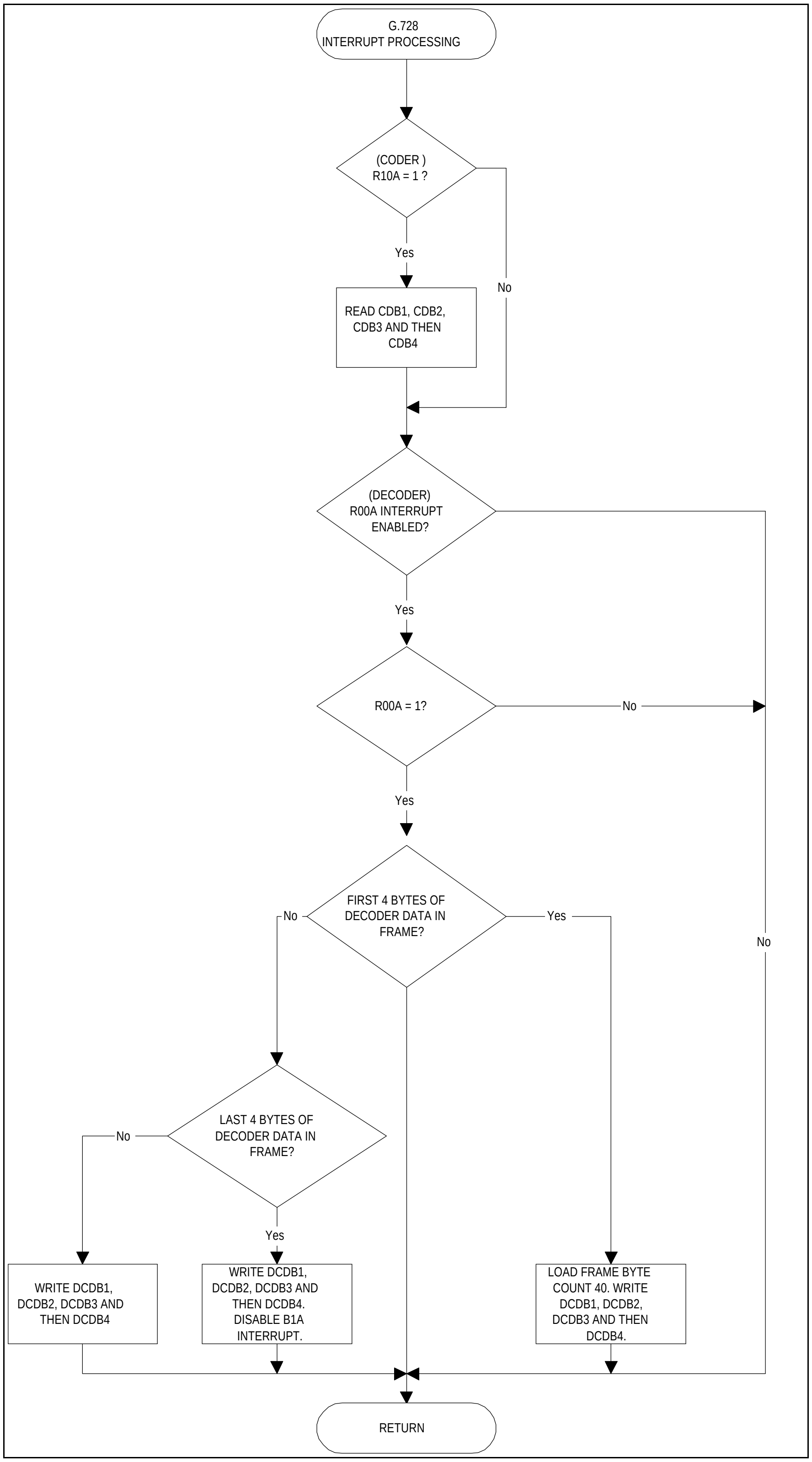

Figure 5-17. G.728 Interrupt Processing

5.7 COMMON CODEC MODES

5.7.1 Handset Mode (SP/HS = 0)

This mode is used for the operation with an telephone handset. A hybrid echo canceller is provided automatically during this mode. To enable Handset mode, reset bit SP/HS.

5.7.2 Headset Mode (FDXEN = 1, HDSET = 1, SP/HS = 1)

This mode is used for the operation with an headset. To select Headset mode, first set bits FDXEN and HDSET, then set bit SP/HS.

5.7.3 Full-Duplex Speakerphone (FDSP) Mode (FDXEN = 1, HDSET = 0, SP/HS = 1)

This mode provides hands-free full-duplex speakerphone operation. A room acoustic echo canceller is provided in this mode. To select FDSP mode, first set bit FDXEN and clear HDSET, then set bit SP/HS.

5.7.4 FDSP and Headset Mode Controls

The host can use the following control bits during FDSP and Headset modes:

MICLVL — Adjust microphone input gain. These two bits are used to adjust the IA microphone input amplifier gain.
00 = 0 dB, 01 = 10 dB (default), 10 = 15 dB, 11 = 20 dB.

MUTEMIC — Mute/enable the microphone input. This bit is used to turn the microphone input on and off.
1 = Mute, 0 = Enable (default).

MUTESPK — Mute/enable the speaker output. This bit is used to turn the speaker output on and off.
1 = Mute, 0 = Enable (default).

VOLDWN — Decrease speaker volume. The host sets VOLDWN to decrease the speaker volume by 1 dB. VOLDWN is automatically cleared after the adjustment is performed. The initial speaker volume setting is -10 dB. The speaker volume is limited to -40 dB.

VOLUP — Increase speaker volume. The host sets VOLUP to increase the speaker volume by 1 dB. VOLUP is automatically cleared after the adjustment is performed. The initial speaker volume setting is -10 dB. The speaker volume is limited to 0 dB.

SPKLVL — Additional speaker digital gain. These two bits allow additional control of the speaker gain.
00 = 0 dB (default), 01 = 6 dB, 10 = 9.5 dB, 11 = 12 dB.

AGCMIC — Enable/disable the microphone AGC. The microphone AGC automatically adjusts the microphone input level. When the talker is silent, the AGC is turned off to prevent the amplification of noise. When speech is detected, the AGC is re-activated. The maximum ACG gain is 18 dB. The AGC reference level and slew rate can be changed using the RAM access utility (see Section 4).
0 = Disable, 1 = Enable (default).

AECDIS — Disable/enable the acoustic echo canceller. For full-duplex speakerphone operation, the AEC should normally be left enabled. However, the AEC performance advantage can be observed by disabling the AEC. During Headset mode, the AEC is always disabled and bit AECDIS is ignored.
0 = Enable (default), 1 = Disable.

5.8 DUAL TONE TRANSMIT CONFIGURATION

The host selects Dual Tone Transmit Configuration by writing 80h to control byte CONF (06:0-7) then setting control bit NEWC (1F:0).

In the Dual Tone Transmit Configuration, the RCSCP2 transmits single or dual frequency tones when enabled by the Tone Transmit bit, DTTX (0D:3). Tone frequencies and amplitudes are programmable in the RCSCP2 RAM (Section 4).

5.9 FUNCTIONS AVAILABLE AT ALL TIMES

5.9.1 Programmable Interface Memory Interrupts

The interface memory interrupt feature enables the host to select an interrupt to occur on any combination of bits within an interface memory register.

The Programmable Interrupt Request bit, PIREQ (1F:3), is set by the RCSCP2 whenever the interrupt condition is true. If the Programmable Interrupt Enable bit, PIE (1F:4), is set by the host and the PIREQ bit is set, the RCSCP2 sets the Programmable Interrupt Active bit, PIA (1F:7), and asserts the enabled interrupt request (~IRQ). The host must reset the PIREQ bit after servicing the interrupt.

An interrupt may occur only within a single interface memory register based upon any combination of bits. For example, the host may select register 0Bh and generate an interrupt whenever bit 0B:1 is set, but may not select bit 0E:2 to generate an interrupt. The register is selected by specifying the Interrupt Address, ITADRS (08:0-4).

The Interrupt Bit Mask register, ITBMSK (09:0-7), selects the bits to be tested in the interface memory register specified by ITADRS. For example, if ITBMSK is equal to FFh, all the bits are selected; if ITBMSK is equal to 0Fh, the four least significant bits are selected.

There are two operating modes (AND or OR) with each mode having four trigger options. The AND/OR Bit Mask Function bit, ANDOR (08:5), selects the operating mode. The Interrupt Triggering bits, TRIG (08:6-7), select the triggering option.

5.9.2 Programmable General Purpose Outputs

Four general purpose output (GPO) lines are programmable by the host. The outputs are controlled by bits GPO4-GPO7 (0F:4-7).

5.10 POWER-ON/RESET SELF-TEST

After Power-on or Reset, the RCSCP2 enters into a self-test and calculates checksums on ROM, RAM and multiplier sections. The results of the checksums and ASCII values corresponding to the RCSCP2 device part number and code revision letter are written to the interface memory registers 10h through 19h approximately 17 milliseconds after Power-on/Reset signal goes off (see Table 5-8). The contents remain in these registers for about 4.0 ms or until register 10 is read by the host.

Table 5-8. Power-On Reset Self-Test Values

Contents	Register (Hex)	Value (Hex)
Multiplier checksum upper word	19	46
Multiplier checksum lower word	18	EE
RAM checksum upper word	17	07
RAM checksum lower word	16	04
ROM checksum upper word	15	39
ROM checksum lower word	14	34
RCSCP2 device number upper word	13	30
RCSCP2 device number lower word	12	33
ASCII value for " " (space)	11	20
RCSCP2 code revision	10	41

The self-test results can also be read using the RAM access utility as follows:

Contents	CR	IO	ADD	Hex Value in Registers 0,1
RAM checksum	0	1	9A	0704
Multiplier checksum	0	1	9B	46EE
ROM checksum	0	1	9C	3934
RCSCP2 code revision	0	1	9D	2041
RCSCP2 device number	0	1	9E	3033

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6. DESIGN CONSIDERATIONS

Good engineering practices must be followed when designing a printed circuit board (PCB) containing the RCSCP2 device. Suppression of noise is essential to the proper operation and performance of the RCSCP2 device as well as interfacing modem, and audio circuits.

Two aspects of noise in an OEM board design containing the RCSCP2 device must be considered: on-board/off-board generated noise that can affect analog signal levels and analog-to-digital conversion (ADC)/digital-to-analog conversion (DAC), and on-board generated noise that can radiate off-board. Both on-board and off-board generated noise that is coupled on-board can affect interfacing signal levels and quality, especially in low level analog signals. Of particular concern is noise in frequency ranges affecting RCSCP2, modem and audio circuit performance.

On-board generated electromagnetic interference (EMI) noise that can be radiated or conducted off-board is a separate, but equally important, concern. This noise can affect the operation of surrounding equipment. Most local governing agencies have stringent certification requirements that must be met for use in specific environments. In order to minimize the contribution of the circuit design and PCB layout to EMI, the designer must understand the major sources of EMI and how to reduce them to acceptable levels.

Proper PC board layout (component placement and orientation, signal routing, trace thickness and geometry, etc.), component selection (composition, value, and tolerance), interface connections, and shielding are required for the board design to achieve desired performance and to attain EMI certification.

All the aspects of proper engineering practices are beyond the scope of this document. The designer should consult noise suppression techniques described in technical publications and journals, electronics and electrical engineering text books, and component supplier application notes. Seminars addressing noise suppression techniques are often offered by technical and professional associations as well as component suppliers.

The following guidelines are offered to specifically help achieve stated performance, minimize audible noise for audio circuit use, and to minimize EMI generation.

6.1 PC BOARD LAYOUT GUIDELINES

6.1.1 General Principles

1. Provide separate digital, analog, and DAA sections on the board.
2. Keep digital and analog components and their corresponding traces as separate as possible and confined to defined sections.
3. Keep high speed digital traces as short as possible.
4. Keep sensitive analog traces as short as possible and separated from digital signals.
5. Provide proper power supply distribution, grounding, and decoupling.
6. Provide separate digital ground, analog ground, and chassis ground (if appropriate) planes.
7. Provide wide traces for power and critical signals.
8. Position digital circuits near the host bus or serial DTE connection and position the DAA circuits near the telephone line connections.

6.1.2 Component Placement

1. From the system circuit schematic,
   a) Identify the digital, analog, DAA, and audio interface circuits and their components, as well as external signal and power connections.
   b) Identify the digital, analog, mixed digital/analog components within their respective circuits.
   c) Note the location of power and signals pins for each device (IC).
2. Roughly position digital, analog, DAA, and audio interface circuits on separate sections of the board. Keep the digital and analog components and their corresponding traces as separate as possible and confined to their respective sections on the board. Typically, the digital circuits will cover one-half of the board, analog circuits will cover one-fourth of the board, and the DAA will cover one-fourth of the board. **NOTE:** While the DAA is primarily analog in nature, it also has many

control and status signals routed through it. A DAA section is also governed by local government regulations covering subjects such as component spacing, high voltage suppression, and current limiting.

3. Once sections have been roughly defined, place the components starting with the connectors and jacks.
   a) Allow sufficient clearance around connectors and jacks for mating connectors and plugs.
   b) Allow sufficient clearance around components for power and ground traces.
   c) Allow sufficient clearance around sockets to allow the use of component extractors.
4. First, place the mixed analog/digital components (e.g., RCSCP2 and modem devices and interfacing components).
   a) Orient the components so pins carrying digital signals extend onto the digital section and pins carrying analog signals extend onto the analog section as much as possible.
   b) Position the components to straddle the border between analog and digital sections.
5. Place all analog components.
   a) Place the analog circuitry, including the DAA, on the same area of the PCB.
   b) Place the analog components close to and on the side of board containing the RBIAS, LINEIN, LINEOUT, MICIN, SPKP, SPKM, VC, and VREF signals.
   c) Avoid placing noisy components and traces near the RBIAS, LINEIN, LINEOUT, MICIN, SPKP, SPKM, VC, and VREF lines.
   d) RBIAS is extremely sensitive to noise; ensure that leads are short and are separated from noise sources, especially digital signals.
   e) For serial DTE models, place receivers and drivers for DTE EIA/TIA-232-E serial interface signals close to the connectors and away from traces carrying high frequency clocks in order to avoid/minimize the addition of noise suppression components (i.e., chokes and capacitors) for each line.
6. Place active digital components/circuits and decoupling capacitors.
   a) Place digital components close together in order to minimize signal trace length.
   b) Place 0.1 µF decoupling (bypass) capacitors close to the pins (usually power and ground) of the IC they are decoupling. Make the smallest loop area possible between the capacitor and power/ground pins to reduce EMI.
   c) For parallel host bus models, place host bus interface components close to the edge connector in accordance with the applicable bus interface standard, e.g., use a 2.5-in maximum trace length for ISA bus.
   d) For serial DTE models, place serial DTE interface components near the DTE connector.
   e) Place crystal circuits as close as possible to the devices they drive.
7. Provide a "connector" component, usually a zero ohm resistor or a ferrite bead at one or more points on the PCB to connect one section's ground to another.

6.1.3 Signal Routing

1. Route the RCSCP2 signals to provide maximum isolation between noise sources and noise sensitive inputs. When layout requirements necessitate routing these signals together, they should be separated by neutral signals. The RCSCP2 noise source, neutral, and noise sensitive pins are listed in Table 6-1.
2. Keep digital signals within the digital section and analog signals within the analog section. (Previous placement of isolation traces should prevent these traces from straying outside their respective sections.) Route the digital traces perpendicular to the analog traces to minimize signal cross coupling.
3. Provide isolation traces (usually ground traces) to ensure that analog signals are confined to the analog section and digital traces remain out of the analog section. A trace may have to be narrowed to route it though a mixed analog/digital IC, but try to keep the trace continuous.
   a) Route an analog isolation ground trace, at least 50 mil to 100 mil wide, around the border of the analog section; put on both sides of the PCB.

b) Route a digital isolation ground trace, at least 50 mil to 100 mil wide, and 200 mil wide on one side of the PCB edge, around the border of the digital section.

4. Keep host interface signals (i. e., RS0-RS4, D0-D7, READ#, WRITE#, ~IRQ, and ~RESET) traces at least 10 mil thick (preferably 12 - 15 mil).
5. Keep analog signal (i.e., RBIAS, LINEIN, LINEOUT, MICIN, SPKP, SPKM, VC, and VREF) traces at least 10 mil thick (preferably 12 - 15 mil).
6. Keep all other signal traces as wide as possible, at least 5 mil (preferably 10 mil). Route the signals between components by the shortest possible path (the components should have been previously placed to allow this).
7. Route the traces between bypass capacitors to IC pins, at least 25 mil wide; avoid vias if possible.
8. Gather signals that pass between sections (typically low speed control and status signals) together and route them between sections through a path in the isolation ground traces at one (preferred) or two points only. If the path is made on one side only, then the isolation trace can be kept contiguous by briefly passing it to the other side of the PCB to jump over the signal traces.
9. Avoid right angle (90 degree) turns on high frequency traces. Use smoothed radiuses or 45 degree corners.
10. Minimize the number of through-hole connections (feedthroughs/vias) on traces carrying high frequency signals.
11. Keep all signal traces away from crystal circuits.
12. Distribute high frequency signals continuously on a single trace rather than several traces radiating from one point.
13. Provide adequate clearance (e.g., 60 mil minimum) around feedthroughs in any internal planes in the DAA circuit.
14. Eliminate ground loops, which are unexpected current return paths to the power source.

Table 6-1. RCSCP2 Pin Noise Characteristics

Package	Function	Noise Source	Neutral	Noise Sensitive
68-Pin PLCC	VDD, AVDD, ADVDD		13, 27, 34, 47	
	VSS, AVSS, ADVSS		9, 20, 26, 29, 32, 46, 51, 62	
	Crystal	24, 25		
	Control		23, 43, 59	
	Host Bus		1-8, 11-12, 21, 63-68	
	Audio Interface			30-31, 33, 35, 38, 52-53
	Device Interconnect		10, 22, 28, 39-40, 44-45, 48-50, 54-57	
	GPIO		15-18	
	No Connection (NC)		14, 19, 36-37, 41-42, 58, 60-61	
144-Pin TQFP	VDD, AVDD, ADVDD		6, 27, 46, 58, 77	
	VSS, AVSS, ADVSS		16, 21, 25, 30, 43, 66, 80-81, 97	
	Crystal	73-74		
	Control		40, 72, 94	
	Host Bus		1-5, 7-15, 52-53, 68	
	Audio Interface			19-20, 23-24, 26, 32, 34
	Device Interconnect		36-37, 44-45, 47-50, 71, 79, 86-88, 90	
	GPIO		61-64	
	No Connection (NC)		17-18, 22, 28-29, 31, 33, 35, 38-39, 41-42, 44, 51, 54-57, 59-60, 65, 67, 69-70, 75-76, 79, 82-85, 89, 91-93, 95-96, 98-100	

6.1.4 Power

1. Identify power supply (VDD/AVDD/ADVDD) connections.
2. Place a 10 µF electrolytic or tantalum capacitor in parallel with a ceramic 0.1 µF capacitor between power and ground at one or more points in the digital section. Place one set nearest to where power enters the PCB (edge connector or power connector) and place another set at the furthest distance from where power enters the PCB. These capacitors help to supply current surge demands by the digital circuits and prevent those surges from generating noise on the power lines that may affect other circuits.
3. For 2-layer boards, route a 200-mil wide power trace on two edges of the same side of the PCB around the border of the circuits using the power. (Note that a digital ground trace should likewise be routed on the other side of the board.)
4. Generally, route all power traces before signal traces.

6.1.5 Ground Planes

1. In a 2-layer design, provide digital and analog ground plane areas in all unused space around and under digital and analog circuit components (exclusive of the DAA), respective, on both sides of the board, and connect them such a manner as to avoid small islands. Connect each ground plane area to like ground plane areas on the same side at several points and to like ground plane areas on the opposite side through the board at several points. Connect all DGND pins to the digital ground plane area and AGND pins to the analog ground plane area. Typically, separate the collective digital ground plane area from the collective analog ground plane area by a fairly straight gap. There should be no inroads of digital ground plane area extending into the analog ground plane area or visa versa.
2. In a 4-layer design, provide separate digital and analog ground planes covering the corresponding digital and analog circuits (exclusive of the DAA), respectively. Connect all DGND pins to the digital ground plane and AGND pins to the analog ground plane. Typically, separate the digital ground plane from the analog ground plane by a fairly straight gap.
3. In a design which needs EMI filtering, define an additional “chassis” section adjacent to the bracket end of a plug-in card. Most EMI components (usually ferrite beads/capacitor combinations) can be positioned in this section. Fill the unused space with a chassis ground plane, and connect it to the metal card bracket and any connector shields/grounds.
4. Keep the current paths of separate board functions isolated, thereby reducing the current's travel distance. Separate board functions are: host interface, digital (SRAM, EPROM, RCSCP2), and audio. Power and ground for each of these functions should be separate islands connected together at the power and ground source points only.
5. Connect grounds together at only one point, if possible, using a ferrite bead. Allow other points for grounds to be connected together if necessary for EMI suppression. For ISA bus board design, include a zero ohm resistor between digital ground and the PC mounting bracket to allow connecting digital ground to the bracket if needed.
6. Keep all ground traces as wide as possible, at least 25 mil to 50 mil.
7. Keep the traces connecting all decoupling capacitors to power and ground at their respective ICs as short and as direct (i.e., not going through vias) as possible.

6.1.6 Crystal Circuit

1. Keep all traces and component leads connected to crystal input and output pins (i.e., XTLI and XTLO) short in order to reduce induced noise levels and minimize any stray capacitance that could affect the crystal oscillator. Keep the XTLO trace extremely short with no bends greater than 45 degrees and containing no vias since the XTLO pin is connected to a fast rise time, high current driver.
2. Where a ground plane is not available, such as in a 2-layer design, tie the crystal capacitors ground paths using separate short traces (as wide as possible) with minimum angles and vias directly to the corresponding device digital ground pin nearest the crystal pins.
3. Connect crystal cases(s) to ground (if applicable).
4. Place a 100-ohm (typical) resistor between the XTLO pin and the crystal/capacitor node.
5. Connect crystal capacitor ground connections directly to GND pin on the RCSCP2 device. Do not use common ground plane or ground trace to route the capacitor GND pin to the corresponding RCSCP2 GND pin.

6.1.7 Telephone and Local Handset Interface

1. Place common mode chokes in series with Tip and Ring for each connector.
2. Decouple the telephone line cables at the telephone line jacks. Typically, use a combination of series inductors, common mode chokes, and shunt capacitors. Methods to decouple telephone lines are similar to decoupling power lines, however, telephone line decoupling may be more difficult and deserves additional attention. A commonly used design aid is to place footprints for these components and populate as necessary during performance/EMI testing and certification.
3. Place high voltage filter capacitors (.001 µF @1KV) from Tip and Ring to digital ground.

6.1.8 Optional Configurations

Because fixed requirements of a design may alter EMI performance, guidelines that work in one case may deliver little or no performance enhancement in another. Initial board design should, therefore, include flexibility to allow evaluation of optional configurations. These optional configurations may include:

1. Chokes in Tip and Ring lines replaced with jumper wires as a cost reduction if the design has sufficient EMI margin.
2. Various grounding areas connected by tie points (these tie points can be short jumper wires, solder bridges between close traces, etc.).
3. EIA/TIA-232 cable ground wire or cable shielding connected on the board or floated.
4. Develop two designs in parallel; one based on a 2-layer board and the other based on a 4-layer board. During the evaluation phase, better performance of one design over another may result in quicker time to market.

6.2 CRYSTAL SPECIFICATIONS

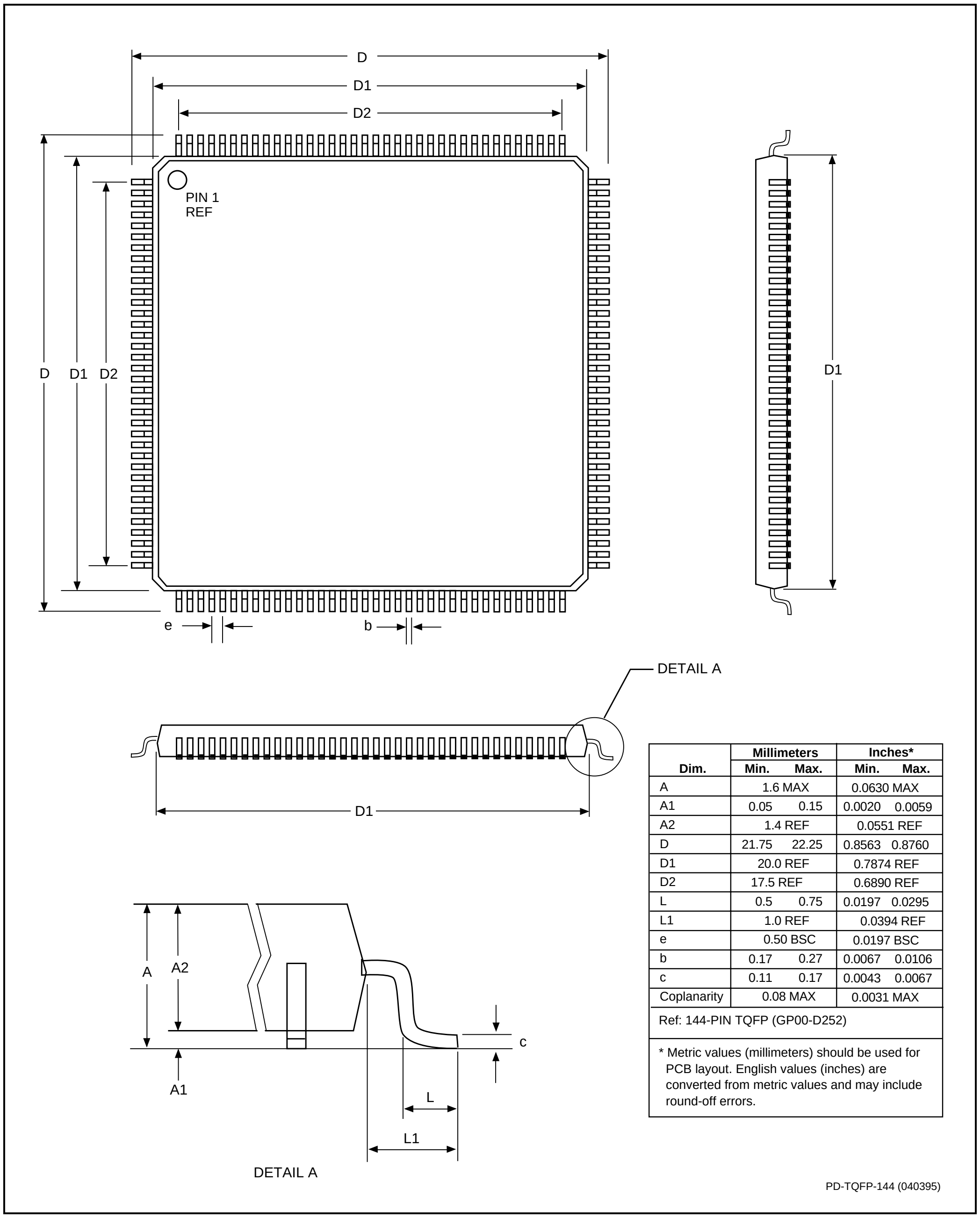
The specifications and recommended suppliers for crystals are listed in Table 6-2.

Table 6-2. Crystal Specifications

Characteristic	Value
Electrical	
Frequency	35.328 MHz nom.
Frequency Tolerance	±40 ppm (C_L = 16.5 and 19.5 pF)
Frequency Stability	
vs. Temperature	±45 ppm (0°C to 70°C)
vs. Aging	±15 ppm/5 years
Oscillation Mode	Third overtone
Calibration Mode	Parallel resonant
Load Capacitance, C_L	18 pF nom.
Shunt Capacitance, C_O	6 pF max.
Series Resistance, R_1	35 Ω max. @20 nW drive level
Drive Level	100µW correlation; 500µW max.
Operating Temperature	0°C to 70°C
Storage Temperature	–40°C to 85°C
Mechanical	
Dimensions (L x W x H)	11.05 x 4.65 x 13.46 mm
Mounting	Through Hole
Holder Type	HC-49/U
Suggested Suppliers	
	ILSI America Kirkland, WA 425/828-4866
Notes 1. Characteristics @ 25°C unless otherwise noted.	

7. PACKAGE DIMENSIONS

The package dimensions are shown in Figure 7-1 (144-pin TQFP).



Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A	1.6 MAX		0.0630 MAX	
A1	0.05	0.15	0.0020	0.0059
A2	1.4 REF		0.0551 REF	
D	21.75	22.25	0.8563	0.8760
D1	20.0 REF		0.7874 REF	
D2	17.5 REF		0.6890 REF	
L	0.5	0.75	0.0197	0.0295
L1	1.0 REF		0.0394 REF	
e	0.50 BSC		0.0197 BSC	
b	0.17	0.27	0.0067	0.0106
c	0.11	0.17	0.0043	0.0067
Coplanarity	0.08 MAX		0.0031 MAX	

Ref: 144-PIN TQFP (GP00-D252)

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

Figure 7-1. Package Dimensions - 144-Pin TQFP

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INSIDE BACK COVER NOTES

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